

L64704 Satellite Decoder

Technical Manual

May 1997



Order Number I14010.A

Document DB14-000026-01, Second Edition (May 1997)

This document describes Revision A of LSI Logic Corporation's L64704 Satellite Decoder and will remain the official reference source for all revisions of this product until rescinded by an update.

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Preface

This book is the primary reference and technical manual for the L64704 Satellite Decoder. It contains a complete functional description for the L64704 and includes complete physical and electrical specifications for the L64704.

Audience

This document assumes that you have some familiarity with digital satellite communications, microprocessors, and related support devices. The people who benefit from this book are:

- ◆ Engineers and managers who are evaluating the L64704 for possible use in a digital satellite receiver
 - ◆ Engineers who are designing the L64704 into a digital satellite receiver
-

Organization

This document has the following chapters and appendix:

- ◆ [Chapter 1, Introduction](#), defines the general characteristics and capabilities of the L64704 Satellite Decoder.
- ◆ [Chapter 2, L64704 Signal Definitions](#), describes the characteristics of the L64704 signals that are used to interface with an external channel and microcontroller.
- ◆ [Chapter 3, L64704 Registers](#), provides a summary of the registers and tables in the L64704.
- ◆ [Chapter 4, Channel Interfaces and Data Control](#), discusses the Input Channel and Output Channel interfaces and the circuitry that supports them.
- ◆ [Chapter 5, Demodulator Module Functional Description](#), describes the operation of the Demodulator portion of the Satellite Decoder.

- ◆ [Chapter 6, Decoding Pipeline Synchronization](#), discusses the mechanism for synchronizing the internal decoder modules to the incoming data stream.
- ◆ [Chapter 7, The FEC Decoder Pipeline](#), describes the various logic modules that comprise the FEC decoding pipeline.
- ◆ [Chapter 8, L64704 Specifications](#), describes the electrical and mechanical characteristics of the L64704.
- ◆ [Appendix A, Programming the L64704 Using the Serial Bus Protocol](#), provides information on how to program the L64704 using its Serial Bus protocol.
- ◆ [Appendix B, L64704 Application Notes](#), provides application information on connecting the L64704 in your circuit and programming it to meet your needs.
- ◆ [Appendix C, Oscillator Cells](#), provides information on the oscillator cells used in the L64704, and how to design oscillators using these cells.

**Related
Publications**

L64002 MPEG-2 Audio/Video Decoder Technical Manual,
Order No. I14011

L64007 MPEG-2, DVB and TSAT Transport Demultiplexer Technical Manual, Document No. DB14-000007-00

European Digital Video Broadcast Standard, DTVB 1110 Revision 7.
This document is available from:

DVB Project Office
European Broadcasting Union
Ancienne Route, 17A
Grand Saconnex
Geneva, Switzerland

**Conventions
Used in This
Manual**

The first time a word or phrase is defined in this manual, it is *italicized*.

The following signal naming conventions are used throughout this manual:

- ◆ A level-significant signal that is true or valid when the signal is LOW always has an overbar ($\overline{\quad}$) over its name.
- ◆ An edge-significant signal that initiates actions on a HIGH-to-LOW transition always has an overbar ($\overline{\quad}$) over its name.

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix "0x" before the number—for example, 0x32CF. Binary numbers are indicated by a subscripted "2" following the number—for example, 0011.0010.1100.1111₂.

Operations on registers are referred to using the binary numbers 0 and 1. Output signal levels are referred to by the designations HIGH and LOW. Example: Set the XCTR0 register bit to 1 to force the XCTR_OUT0 pin HIGH.

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Chapter 1

Introduction

This chapter introduces the L64704 Satellite Decoder from LSI Logic. The L64704 is designed specifically to meet the needs of satellite broadcast digital TV.

The sections in this chapter are:

- ◆ [Section 1.1, “General Description,”](#) provides an overview of the architecture of the L64704 Satellite Decoder.
 - ◆ [Section 1.2, “Typical Application,”](#) describes how the L64704 is used in a typical satellite decoder system.
 - ◆ [Section 1.3, “Features Summary,”](#) summarizes the main features of the L64704.
-

1.1 General Description

The L64704 Satellite Decoder contains two main blocks: a BPSK/QPSK Demodulator and a Concatenated FEC decoder.

The BPSK/QPSK module performs binary and quadrature phase-shift keying (BPSK/QPSK) demodulation, a method of extracting a digital signal from a phase-modulated analog signal. The BPSK/QPSK module is designed specifically for a satellite broadcast digital TV receiver, and is compliant with the European digital video broadcast (DVB) standard (DTVB 1110 Rev. 7).

The FEC Decoder pipeline is a complete concatenated Forward Error Correction decoder that utilizes a Viterbi inner code and a Reed-Solomon outer code. The FEC decoding pipeline also contains all of the necessary synchronization, deinterleaving, and scrambling functions for a complete decoding solution.

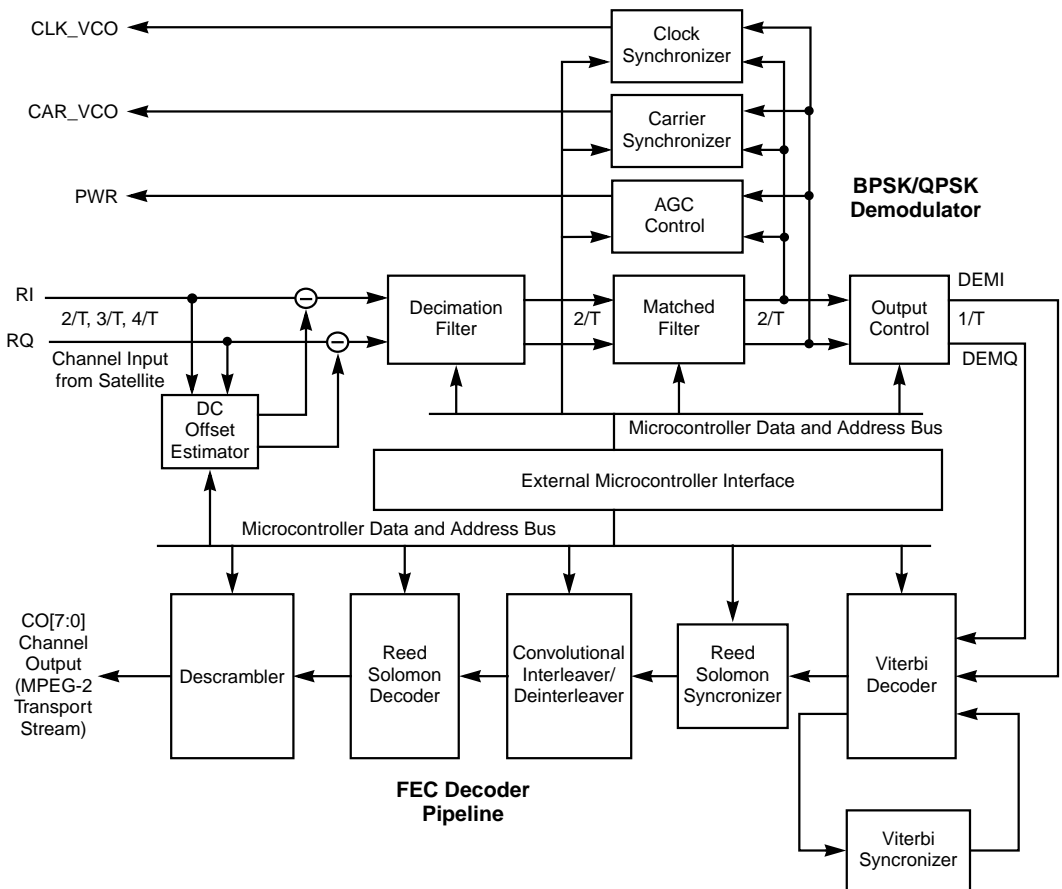
The L64704 is compliant with specifications of the “Baseline Modulation/Channel Coding System” by the Digital Video Broadcast

(DVB) Association. LSI Logic fabricates the L64704 using its LCB500K, 3.3-volt, 0.5-micron, HCMOS process technology.

The L64704 provides maximum integration and flexibility for system designers at a minimum cost. The number of external components required to build a system is minimal; only a dual operational amplifier and passive resistors and capacitors are needed for the implementation of the clock and carrier loop filters.

Figure 1.1 shows a block diagram of the L64704.

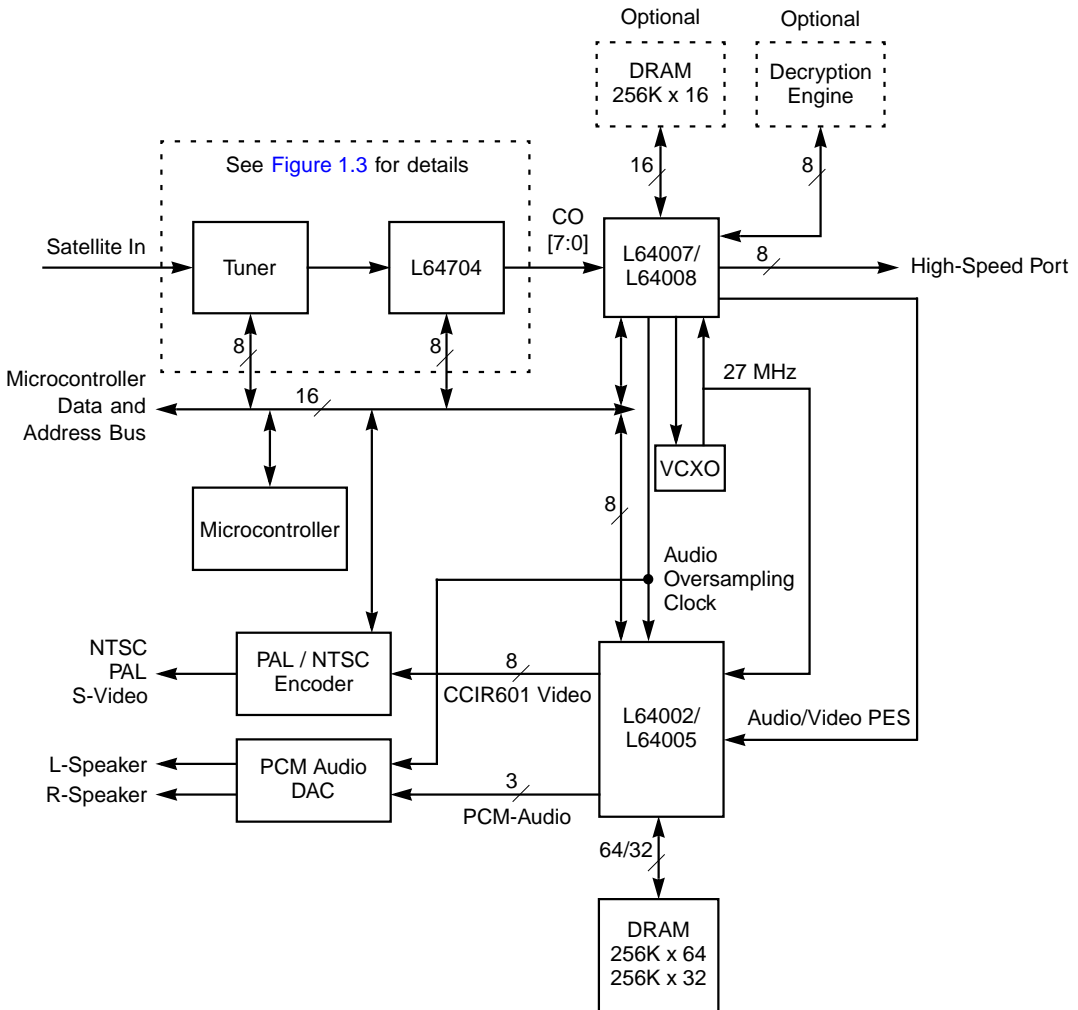
Figure 1.1
L64704 Block Diagram



1.2
Typical
Application

A typical application of the L64704 is satellite digital TV reception according to the DVB 1110 Rev. 7 standard. Figure 1.2 shows the L64704 Satellite Decoder in a typical Satellite Receiver Set-Top Decoder box.

Figure 1.2
 Set-Top Decoder Box
 Block Diagram



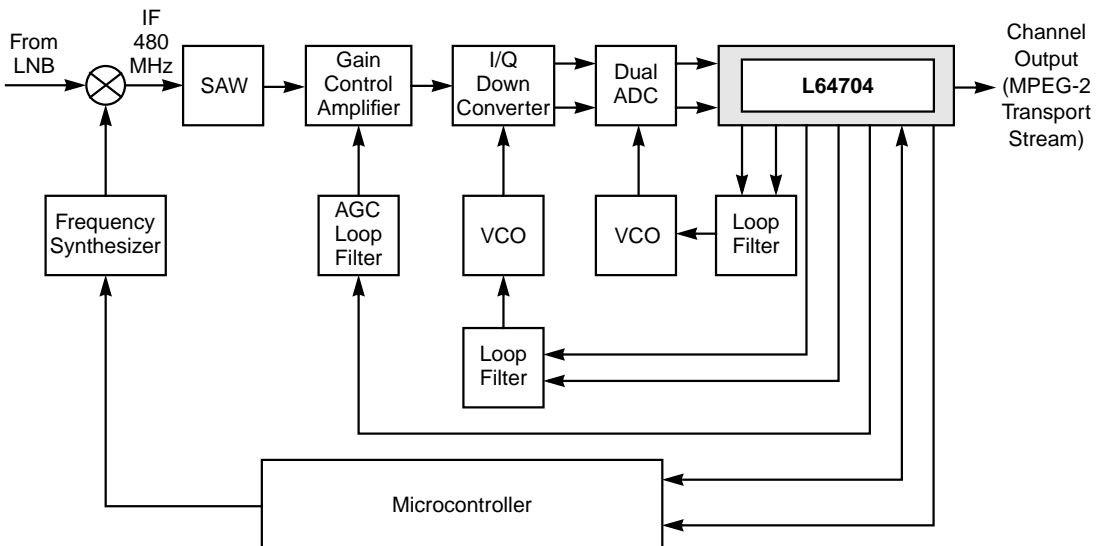
LSI Logic offers circuits that make up the most complex portions of the logic found in a Set-Top Decoder box. These circuits include the:

- ◆ L64704 Satellite Decoder
- ◆ L64007 MPEG-2 Transport Demultiplexer
- ◆ L64002 MPEG-2 Audio/Video Decoder

For more information on the other integrated circuits in the Set-Top Decoder box, see their associated manuals.

Figure 1.3 shows a block diagram of a satellite tuner that includes the L64704.

Figure 1.3
Typical Receiver Block
Diagram with L64704



The receiver block receives the microwave channel data from the satellite dish, demodulates and decodes it, and outputs an MPEG-2 transport stream.

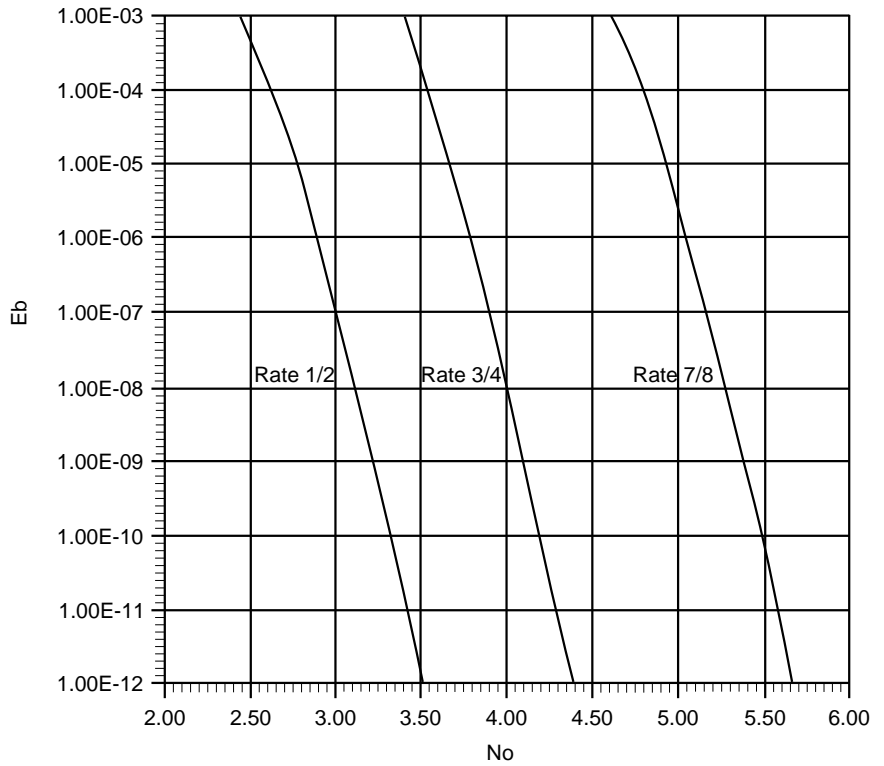
1.3 Features Summary

This section summarizes the main features of the L64704. Subsequent chapters describe these features in more detail.

- ◆ Variable BPSK/QPSK demodulation from 2 to 62.5 Mbit/s
- ◆ Matched filter (square root raised cosine filter, roll-off factor of 35%)
- ◆ Decimation filters for input oversampling ratios of 2/T, 3/T, and 4/T
- ◆ Clock synchronization
- ◆ Carrier synchronization featuring a frequency sweep capability for signal acquisition
- ◆ Power estimation for AGC control
- ◆ Internal DC offset control
- ◆ Programmable Viterbi decoder module for rates 1/2, 2/3, 3/4, 5/6, 7/8
- ◆ (204/188) Reed-Solomon decoder
- ◆ Auto synchronization for Viterbi decoder
- ◆ Programmable synchronization for Deinterleaver, Reed-Solomon Decoder, and Descrambler
- ◆ FEC module flags uncorrectable frames by setting the ninth bit of the MPEG Transport packet.
- ◆ Bit Error monitoring for channel performance measurements
- ◆ Depth 12 deinterleaver
- ◆ Serial host interface compatible with the LSI Logic Serial Control bus interface
- ◆ Power down mode

[Figure 1.4](#) shows a performance graph for the L64704 Satellite Decoder.

Figure 1.4
Concatenated
Decoding
Performance for
L64704



Chapter 2

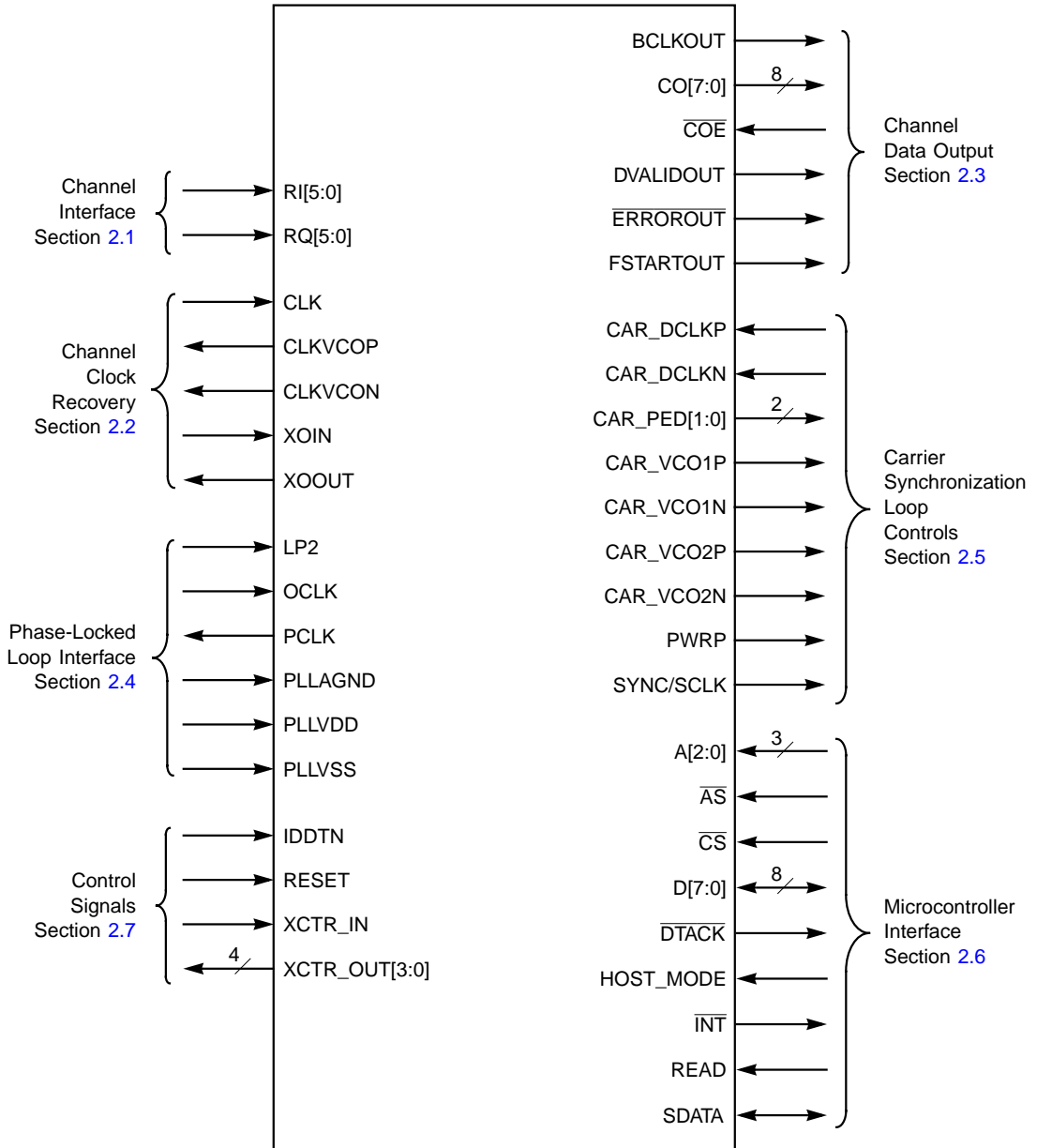
L64704 Signal Definitions

This chapter describes the signals that comprise the L64704 Satellite Decoder's interface to other components. This chapter is divided into seven sections that describe the various buses:

- ◆ [Section 2.1, "Channel Interface,"](#) describes the input channel interface to the L64704.
- ◆ [Section 2.2, "Channel Clock Recovery,"](#) lists the signals that make up the input channel clock recovery circuitry.
- ◆ [Section 2.3, "Channel Data Output Interface,"](#) describes the signals that connect the channel data outputs to the MPEG demultiplexer.
- ◆ [Section 2.4, "Phase-Locked Loop Interface,"](#) lists the signals that are used to connect the L64704 to an external Phase-Locked Loop.
- ◆ [Section 2.5, "Carrier Synchronizer Loop Controls,"](#) provides a list of the signals that are used to synchronize the I/Q Down Converter circuitry.
- ◆ [Section 2.6, "Microcontroller Interface,"](#) shows the signals that are used to connect the L64704 to an external microcontroller.
- ◆ [Section 2.7, "Control Signals,"](#) describes the various signals that are necessary for the operation of the L64704, but do not fit into any of the categories above.

[Figure 2.1](#) shows the logic symbol for the L64704.

Figure 2.1
L64704 Logic Diagram



2.1 Channel Interface

The Channel Interface is the input path to the L64704 Satellite Decoder. The two signal buses RI[5:0] and RQ[5:0] are the I and Q streams from the satellite tuner circuit. The CLK signal discussed in the Channel Clock Recovery section is used to strobe in the data signals. The Channel Interface is discussed in [Section 4.2, “Channel Data Input Interface.”](#)

RI[5:0]	I Channel Data Received I Channel data input bus.	Input
RQ[5:0]	Q Channel Data Received Q Channel data input bus.	Input

2.2 Channel Clock Recovery

The Channel Clock Recovery logic is the logic that recovers the clock for the Channel Interface. Channel Clock recovery is discussed in [Section 5.5, “Channel Clock Recovery.”](#)

CLK	RI/Q Input Clock CLK is a positive, edge-triggered clock that is used to strobe in input data. It is not used anywhere else in the L64704, and does not propagate past the Channel Interface.	Input
CLK_VCOP/N	Clock Loop VCO Control These two differential signals are the Positive and Negative Sigma Delta ($\Sigma\Delta$) modulated output used to control the Channel Clock VCO frequency.	Output
XOIN	Crystal Oscillator In The XOIN pin is the crystal oscillator or external reference clock input.	Input
XOOUT	Crystal Oscillator Out The XOOUT pin is the crystal oscillator output pin.	Output

**2.3
Channel Data
Output Interface**

The Channel Data Output Interface is the output path from the L64704. It is typically connected to the input of the Transport Demultiplexer in a set-top decoder application. The Channel Data Output Interface is discussed in [Section 4.3, "Channel Data Output Interface."](#)

BCLKOUT	Byte Clock Out	Output
	The BCLKOUT output signal is a strobe that indicates valid data bytes on the CO[7:0] bus when the L64704 is in Parallel Channel Output mode. The BCLKOUT signal cycles once per every valid output data byte and is used by the Transport Demultiplexer to latch output data from the L64704 at the BCLKOUT rate (rather than at the OCLK rate). BCLKOUT must be disregarded in Serial Channel Output mode.	
CO[7:0]	Channel Data Out	Output
	These signals form the decoded output data port. In Parallel Channel Output mode (OF = 1, Group 4, APR 12) the L64704 outputs the channel data as 8-bit wide parallel data on CO[7:0]. In Serial Channel Output mode (OF = 0) the L64704 outputs the channel data as serial data on CO0. It is latched on every byte or bit clock cycle. The chronological ordering in Serial Channel output mode is MSB oldest, LSB newest.	
$\overline{\text{COE}}$	Channel Output Enable	Input
	When asserted, $\overline{\text{COE}}$ enables the CO[7:0], $\overline{\text{ERROROUT}}$, and FSTARTOUT pins. DVALIDOUT is unaffected by the $\overline{\text{COE}}$ pin and operation of the decoder continues regardless of the state of this pin.	
DVALIDOUT	Valid Data Out	Output
	DVALIDOUT indicates that CO[7:0] contains the corrected channel data. New data is valid on the output when DVALIDOUT is HIGH. DVALIDOUT is not asserted during the propagated check and GAP bytes. This pin is set LOW after the FEC_RST register bit (Group 4, APR 36) is asserted.	
$\overline{\text{ERROROUT}}$	Error Detection Flag	Output
	The L64704 asserts the $\overline{\text{ERROROUT}}$ pin to flag uncorrectable errors. The L64704 asserts the $\overline{\text{ERROROUT}}$ signal at the beginning of any frame that contains an uncorrectable error, and deasserts it at the end of the	

frame (if the error condition is removed). $\overline{\text{ERROROUT}}$ is exactly aligned with the output data stream. This pin is set HIGH after the FEC_RST register bit (Group 4, APR 36) is asserted.

FSTARTOUT **Frame Start Output** **Output**
The L64704 asserts FSTARTOUT during the first bit of every frame with valid data in Serial Channel Output mode and during the first byte in Parallel Channel Output mode. FSTARTOUT is valid only when DVALIDOUT is HIGH. This pin is set LOW after the FEC_RST register bit (Group 4, APR 36) is asserted.

2.4 Phase-Locked Loop Interface

The Phase-Locked Loop (PLL) circuitry multiplies the Channel Clock Recovery circuit SCLK signal by 2, 3, or 4 times the symbol rate, based on the Viterbi code rate. The output from the PLL (PCLK) is brought back into the L64704 on the OCLK pin to clock the FEC Decoder logic. Use of the PLL is discussed in [Section 4.4, “PLL Clock Generation.”](#)

LP2 **Input to VCO** **Input**
This pin is the input to the internal voltage controlled oscillator. It is normally connected to the output of an external RC timing circuit.

OCLK **Decoder Clock** **Input**
The positive edge of OCLK is a positive, edge-triggered clock. The L64704 internally processes data (Viterbi decoder, Synchronization, Descrambler, Deinterleaver, Reed-Solomon Decoder) based on OCLK. All data outputs (DVALIDOUT, $\overline{\text{ERROROUT}}$, FSTARTOUT, CO[7:0]) are referenced to OCLK. OCLK is independent of CLK.

PCLK **PLL Clock Output** **Output**
The L64704's internal PLL clock synthesis module generates the clock signal PCLK. The PLL is driven by the SCLK internal signal (QPSK symbol clock). The PLL clock synthesis module can be configured to generate a PCLK rate that is appropriate for all Viterbi code rates specified under the DVB standard.

PLLAGND **PLL Analog Ground** **Input**
Analog ground pin for the PLL module. This pin is normally connected to the system ground plane.

PLLVD	PLL Power	Input
	Power supply pin for the PLL module. This pin is normally connected to the system power (V_{DD}) plane.	
PLLVS	PLL Ground	Input
	Power supply pin for the PLL module. This pin is normally connected to the system ground plane.	

2.5 Carrier Synchronizer Loop Controls

Carrier Synchronizer Loop controls are used to synchronize the I/Q Down Converter circuitry. Carrier Synchronizer Loop controls are discussed in [Section 5.6, “Carrier Synchronizer.”](#)

CAR_DCLKP/N
VCO Prescaler Input **Input**
The CAR_DCLK pins are differential inputs for the pre-scaled (divided) Carrier VCO clock (typically = VCO frequency / 32).

CAR_PED[1:0]
Carrier Phase Error Detector **Output**
These pins are the 2-bit outputs from the Phase Error Detector. You use the CAR_PED outputs for carrier loop implementation in combination with an external digital to analog converter. It should be used when operating at rates less than 5 Mbaud.

CAR_VCO1P/N
Carrier Loop VCO Control 1 **Output**
When CAR_OUT_SEL (Group 4, APR 33) is set to 0, these pins are the Positive/Negative $\Sigma\Delta$ modulated outputs that control the carrier VCO frequency. CAR_VCO1P/N feed external RC circuit number 1. A LOW output decreases the carrier VCO frequency. A HIGH output increases the carrier VCO frequency. A high impedance level maintains the carrier VCO frequency. When CAR_OUT_SEL is set to 1, these pins carry the CAR_PED.2 and CAR_PED.3 signals.

CAR_VCO2P/N
Carrier Loop VCO Control 2 **Output**
When CAR_OUT_SEL (Group 4, APR 33) is set to 0, these pins are the Positive/Negative $\Sigma\Delta$ modulated outputs that control the carrier VCO frequency. CAR_VCO2P/N feed external RC circuit number 2. A LOW output decreases the carrier VCO frequency. A

HIGH output increases the carrier VCO frequency. A high impedance level maintains the carrier VCO frequency. When CAR_OUT_SEL is set to 1, these pins carry the CAR_PED.4 and CAR_PED.5 signals.

PWRP	Power Control	Output
	The power control signal is the positive $\Sigma\Delta$ modulated output used for power control. This signal can drive an external passive RC filter that feeds the gain control stage.	
SYNC/SCLK	Synchronization Status Flag	Output
	When the SYNC/SCLK bit (Group 4, APR 14) is set to 0, the SYNC/SCLK pin indicates the synchronization status for one of three synchronization modules in the L64704 (Viterbi Decoder sync, DI/RS sync, Descrambler sync). When HIGH the SYNC/SCLK output indicates the synchronization has been achieved for the chosen sync module. When LOW, the SYNC/SCLK output indicates an out-of-synchronization condition.	
	When the SYNC/SCLK bit is set to 1, the SYNC/SCLK pin carries the SCLK signal that is used to clock the external DAC during low baud rate operation. See Section 5.6.2.3, “Low Baud Rate Operation” for more information.	

**2.6
Microcontroller
Interface**

The Microcontroller Interface connects the L64704 to a microcontroller.

A[2:0]	Address	Input
	A[2:0] comprise the decoder address bus. The address bus is used in conjunction with an eight-bit data bus D[7:0], a read/write strobe (READ), a chip select strobe (\overline{CS}), and an address strobe (\overline{AS}) to select, read and write internal registers.	
\overline{AS}	Address Strobe	Input
	\overline{AS} is an active-LOW address strobe input. The L64704 latches the address on A[2:0] on the falling edge of \overline{AS} .	
\overline{CS}	Chip Select	Input
	\overline{CS} is an active-LOW chip select strobe input. During a read cycle, the microcontroller must pull \overline{CS} LOW to access the on-chip data registers. The controller should	

latch the data from the L64704 on the rising edge of \overline{CS} . During a write cycle, \overline{CS} must go LOW prior to data being valid from the controller to the L64704. After the data has met the minimum setup time, the microcontroller takes \overline{CS} HIGH to strobe the data. There is a minimum write time to allow for internal synchronization. Setup and hold times are measured with respect to the falling edge of \overline{CS} .

D[7:0]	Data Bus	Bidirectional
	D[7:0] is the bidirectional data bus; it is the input data bus when data is written to the chip and the data output bus when the chip is read in Parallel Host Interface mode (HOST_MODE pin is HIGH). The data lines are 3-stated when not being read or written. When Serial Host Interface mode is selected (HOST_MODE pin is LOW), D0 is used as the Serial Clock signal to synchronize the transfer of serial data on the SDATA pin. The remaining seven bits of the data bus function as the slave address.	
\overline{DTACK}	Data Acknowledge	Output
	Data Acknowledge is an active-LOW output indicating that the transaction on the D[7:0] bus has been completed.	
HOST_MODE	Serial or Parallel Host Interface Select	Input
	When HOST_MODE is LOW, it selects the Serial Host Interface mode; when HIGH, it selects the Parallel Host Interface mode.	
\overline{INT}	Interrupt	Output
	The L64704 asserts \overline{INT} LOW when an internal unmasked interrupt flag is set. \overline{INT} remains asserted as long as the interrupt condition persists and the interrupt flag is not masked.	
READ	Read/Write Strobe	Input
	The microcontroller drives READ HIGH to indicate that the current transaction is a read from the L64704, and LOW to indicate that it is a write to the L64704.	
SDATA	Serial Host Interface Data	Bidirectional
	This bidirectional pin is the data input or output pin when Serial Host Interface mode is selected (HOST_MODE is LOW).	

2.7

Control Signals

These signals control the operation of the L64704. They are not associated with any particular interface.

IDDTN	Test Pin IDDTN is an LSI Logic internal test pin. Connect this pin LOW for normal operation.	Input
RESET	Reset This active-HIGH signal resets all internal data paths. Reset timing is asynchronous to the device clocks. Reset does not affect the configuration registers. It performs the same operation as the reset bits specified in Section 3.6.31, "Group 4, APR 36 External Output Control Bits and Reset Register."	Input
XCTR_IN	Control Input Pin The XCTR_IN pin is an external input control pin. It is sensed by reading the corresponding bit in the Group 3, APR 6 register.	Input
XCTR_OUT[3:0]	Control Output Pins The XCTR_OUT[3:0] pins are external output control pins. They are set by programming the corresponding bits in the Group 4, APR 36 register.	Output

Chapter 3

L64704 Registers

This chapter discusses the L64704 internal registers. It also provides a description of the internal memory mapping and describes how to access these registers from the system interface. This chapter is intended primarily for system programmers who are developing software drivers.

This chapter contains the following sections:

- ◆ [Section 3.1, “L64704 Register Overview,”](#) provides an overview of the registers contained within the L64704.
- ◆ [Section 3.2, “Reset and How It Affects Registers,”](#) describes the three separate methods of resetting the L64704 and how each method affects the registers.
- ◆ [Section 3.3, “Group 0, 1 Address Pointer Register,”](#) describes how to address and use the Address Pointer Register.
- ◆ [Section 3.4, “Group 2 Registers,”](#) provides information on the use of the System Mode and System Status Registers.
- ◆ [Section 3.5, “Group 3 Registers,”](#) describes how to read and use the Status Registers.
- ◆ [Section 3.6, “Group 4 Registers”](#) provides information on programming and using the L64704’s Configuration Registers.

This chapter provides complete information on how to use these registers, but does not provide information on how to program the registers for a specific application. See [Appendix B, “L64704 Application Notes ”](#) for applications information.

3.1 L64704 Register Overview

The L64704 registers and memory resources are divided into five groups: Group 0 through Group 4. Group 0 and 1 contain the Address Pointer Register. This pointer is used to address the registers in Groups 2, 3 and 4. Group 2 addresses the System Status Register when read and the System Mode Register when written. Group 3 contains the status counters, and Group 4 contains the configuration registers (See [Table 3.1](#)).

Table 3.1
Register Overview

Group	Function	Page
0	Address Pointer Register, LSB	3-10
1	Address Pointer Register, MSB	3-10
2	System Mode/Status Registers	3-11
3	Status Registers	3-20
4	Configuration Registers	3-26
5	Reserved	
6	Reserved	
7	Reserved	

[Table 3.2](#) shows the complete Register Map for the L64704 Satellite Decoder.

Table 3.2
Register Map

Group	APR	Bit(s)	R/W	Description	Acronym	Page
0	N/A	7:0	W	Address Pointer Register LSB	APR	3-10
1	N/A	7:0	W	Address Pointer Register MSB	APR	3-10
2	0	7:0	R	System Status Register [7:0]	STS	3-16
		7:0	W	System Mode Register [7:0]	SMR	3-11
	1	7:0	R	System Status Register [15:8]	STS	3-16
		7:0	W	System Mode Register [15:8]	SMR	3-11
3	0	7:0	R	Reed-Solomon Corrected Error Count	CEC[7:0]	3-21
	1	7:0	R	Reed-Solomon Corrected Error Count	CEC[15:8]	3-21
	2	7:0	R	Reed-Solomon Uncorrected Error Count	UEC[7:0]	3-21
	3	7:0	R	Reed-Solomon Uncorrected Error Count	UEC[15:8]	3-21
	4	7:0	R	Viterbi Bit Error Rate Count Low Byte	VBERC[7:0]	3-22
	5	7:0	R	Viterbi Bit Error Rate Count High Byte	VBERC[15:8]	3-22

(Sheet 1 of 4)

Table 3.2 (Cont.)
Register Map

Group	APR	Bit(s)	R/W	Description	Acronym	Page
3	6	7	R	Demodulator Signal to Noise Ratio	Demod_SNR	3-22
		6	R	External Control Bit Input	XCTR_IN	3-22
		5:0	R	Measured VCO Frequency, Upper Bits	CAR_VCOF[13:8]	3-22
	7	7:0	R	Measured VCO Frequency, Lower Byte	CAR_VCOF[7:0]	3-23
	8	7:0	R	AGC Loop Voltage Meter	PWR_LVL[7:0]	3-23
	9	5	R	Carrier Frequency Lock Flag	CAR_LCF	3-23
		4	R	Carrier Phase Lock Flag	CAR_LC	3-23
		3	R	Clock Frequency Lock Flag	CLK_LCF	3-23
		2	R	Stage 3 Synchronization Flag	S3	3-23
		1	R	Stage 2 Synchronization Flag	S2	3-23
		0	R	Stage 1 Synchronization Flag	S1	3-23
10	5:0	R	RI Input Readback	RI	3-25	
11	5:0	R	RQ Input Readback	RQ	3-26	
4	0	5:0	R/W	Phase-Locked Loop Config. Param. N	PLL_N[5:0]	3-28
	1	5:0	R/W	Phase-Locked Loop Config. Param. S	PLL_S[5:0]	3-28
	2	7	R/W	(I, -Q) Symbol Format	IMQ	3-29
		5	R/W	QPSK/BPSK Format Select	QB	3-29
		4:0	R/W	Phase-Locked Loop Config. Param. T	PLL_T[4:0]	3-29
	3	7:5	R/W	Viterbi Code Rate	VCR[2:0]	3-30
		4	R/W	Transport Error Indicator Select	TEI	3-30
		3	R/W	Select SYNC 2 Modified Algorithm	SYNC2_MOD	3-30
		1:0	R/W	VCO Frequency Range for PLL Module	PLL_M[1:0]	3-30
	4	7:0	R/W	Viterbi Maximum Data Bit Count 1	VMDC1[7:0]	3-31
	5	7:0	R/W	Viterbi Maximum Data Bit Count 2, Low	VMDC2[7:0]	3-31
	6	7:0	R/W	Viterbi Maximum Data Bit Count 2, Middle	VMDC2[15:8]	3-31
	7	7:0	R/W	Viterbi Maximum Data Bit Count 2, High	VMDC2[23:16]	3-31
	8	7:0	R/W	Viterbi Maximum Bit Error Count	VMBEC[7:0]	3-32
	9	7:0	R/W	Synchronization Word	Sync[7:0]	3-32
10	7	R/W	Bit Error Rate Monitor	BER	3-33	
	1:0	R/W	Mismatching Bits, Tracking Mode, Sync2	L[1:0]	3-33	

(Sheet 2 of 4)

Table 3.2 (Cont.)
Register Map

Group	APR	Bit(s)	R/W	Description	Acronym	Page
4	11	7	R/W	BCLKOUT Format	BF	3-34
		5:4	R/W	Synchronization Status Select	SSS[1:0]	3-34
		3:2	R/W	Synchronization States, Acquisition Mode	SSA[1:0]	3-34
		1:0	R/W	Synchronization States, Tracking Mode	SST[1:0]	3-34
	12	7:5	R/W	Symbol Size for Viterbi Bypass Mode	BPS[2:0]	3-36
		3	R/W	Descrambler Output Format	OF	3-36
		2:0	R/W	Output Selector, OS[2:0]	OS[2:0]	3-36
	13	7:0	W	Reset for PLL Module	PLL_RESET	3-37
	14	7	R/W	SYNC/SCLK Selector Bit	SYNC/SCLK	3-37
		4	R/W	Functional Outputs 3-stated	F_OUT_HI_Z	3-37
		3	R/W	CLK_LCF_Suppress in Timing Error Detector	CLK_LCF_Suppress	3-37
		2	R/W	Clock Outputs Polarity Swap	CLK_VCO_SWAP	3-37
		1:0	R/W	Decimation Filter Select	CLK_DR[1:0]	3-37
	15	6	R/W	PCLK Bypass	PCLK_BP	3-39
		4	R/W	Power-Down	PD	3-39
		3:0	R/W	Reference Period for Clock AFC	CLK_RP[3:0]	3-39
	16	7:0	R/W	CLK Input Nominal Frequency, Upper	CLK_NF[15:8]	3-40
	17	7:0	R/W	CLK Input Nominal Frequency, Lower	CLK_NF[7:0]	3-40
	18	2:0	R/W	Input Decimation Factor for RI & RQ Inputs	CLK_RATIO[2:0]	3-40
	19	7:0	R/W	Reference Power Level	PWR_REF[7:0]	3-41
	20	2	R/W	Internal DC Offset Compensation on I and Q Signals	INT_DC	3-41
		1:0	R/W	Power Estimation Bandwidth	PWR_BW[1:0]	3-41
	21	7:0	R/W	Scale Factor for DEMI and DEMQ Outputs	SCALE[7:0]	3-42
	22	7:0	R/W	SNR Estimator Threshold	SNR_THS[7:0]	3-42
	23	7:0	R/W	Carrier Loop DC Offset Comp. Value	CAR_OFFSET[7:0]	3-42
	24	3:0	R/W	Reference Period for Carrier Frequency (CAR_DCLKP/N) Measurement	CAR_RP[3:0]	3-43
25	7:0	R/W	Gain of Carrier Loop Filter (P Term)	CAR_KP[7:0]	3-43	
26	7:0	R/W	Gain of Carrier Loop Filter (D Term)	CAR_KD[7:0]	3-43	

(Sheet 3 of 4)

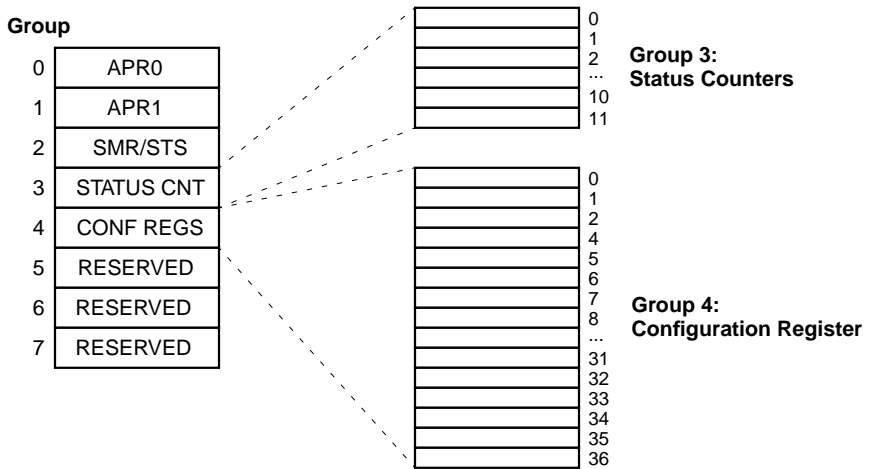
Table 3.2 (Cont.)
Register Map

Group	APR	Bit(s)	R/W	Description	Acronym	Page
4	27	7:0	R/W	Threshold for Carrier Lock Detector	CAR_THSL[7:0]	3-44
	28	7:0	R/W	Sweep Rate for Carrier Sweep	CAR_SWR[7:0]	3-44
	29	5:0	R/W	Upper Sweep Limit for Carrier Sweeping, Upper Bits	CAR_USWL[13:8]	3-44
	30	7:0	R/W	Upper Sweep Limit for Carrier Sweeping, Lower Byte	CAR_USWL[7:0]	3-44
	31	5:0	R/W	Lower Sweep Limit for Carrier Sweeping, Upper Bits	CAR_LSWL[13:8]	3-46
	32	7:0	R/W	Lower Sweep Limit for Carrier Sweeping, Lower Byte	CAR_LSWL[7:0]	3-46
	33	7	R/W	Swap Carrier Sweep Direction	CAR_SWP_SWP	3-46
		6	R/W	CAR_VCO Swap Outputs Polarity	CAR_VCO_SWAP	3-46
		5	R/W	CAR_VCO2N/P Outputs Active or 3-state	CAR_VCO2N/P	3-46
		4	R/W	CAR_VCO1N/P Outputs Active or 3-state	CAR_VCO1N/P	3-46
		3	R/W	Carrier Loop Output Selector	CAR_OUT_SEL	3-46
		2	R/W	Carrier Phase Error Detector Select	CAR_PED_SEL	3-46
		1	R/W	Carrier Loop Open	CAR_OPEN	3-46
		0	R/W	Sweep On/Off for Carrier Loop	CAR_SW	3-46
		34	7:5	R/W	Set to 0	Set to 0
	35	7	R/W	Signal to Noise Estimator On/Off	SNR_EST	3-50
		6	R/W	Constellation Selector	CON_SEL	3-50
		4	R/W	Frequency/Phase Lock Detector Length	FP_LOCK_LEN	3-50
		0	R/W	Input Format Selector	I_FORMAT	3-50
	36	2:5	R/W	External Control Output Bits	XTCR[3:0]	3-51
		1	R/W	QPSK Demodulator Software Reset	DEMOD_RST	3-51
		0	R/W	FEC Decoder Software Reset	FEC_RST	3-51

(Sheet 4 of 4)

Figure 3.1 shows a simplified diagram of the L64704's register file.

Figure 3.1
Register-File
Structure



To reduce the number of memory locations occupied by the L64704 in microcontroller memory, the L64704 uses an Address Pointer Register (APR). The APR has an auto-increment feature that simplifies the initialization procedure and reduces the number of memory cycles needed to read or write the registers. The address pointer and auto-increment feature are used whenever you access Groups 2, 3, and 4. The L64704 automatically points to the next register entry after you complete an access to one of these groups. When configuring or reading the configuration of groups 3 and 4, you will find it easier to initially set APR0 and APR1 to zero and let the auto-increment mechanism step through all the locations within the group.

For example: to access the PLL_N configuration register 0 (Group 4, APR 0), first set APR0 = APR1 = 0₂ by writing a zero to addresses 0 and 1, then set A[2:0] to 100₂. Address A[2:0] selects Group 4 of the six APR groups.

Internally, the L64704 has an 8-bit architecture. Most registers are eight bits wide, while some are either 16- or 24-bits wide. All registers are memory-mapped to the system with 8-bit resolution. When you are accessing a register that is wider than 8 bits, you must read or write two or three 8-bit sections: the least-significant byte (LSB) the middle-significant byte (MB) and the most-significant byte (MSB). Each 8-bit section is assigned a specific address, and therefore requires an individual memory cycle during programming.

3.1.1 Parallel Host Mode Register Operations

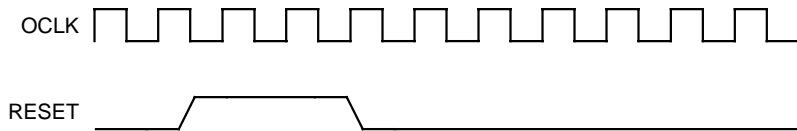
The L64704 is addressable through either a serial or a parallel host interface. The interface used depends on the value of the HOST_MODE pin (HIGH: Parallel Host Interface mode, LOW: Serial Host Interface mode) when the L64704 is reset. The mode, however, cannot be changed once the part is in operation. This section shows the steps required to read and write the L64704's registers when you are in Parallel Host Interface mode. Serial Host Interface mode is discussed in Section 3.1.2, "Programming Using the Serial Interface."

The following diagrams demonstrate read and write operation through the parallel microprocessor interface.

Note: OCLK must run throughout the initialization process.

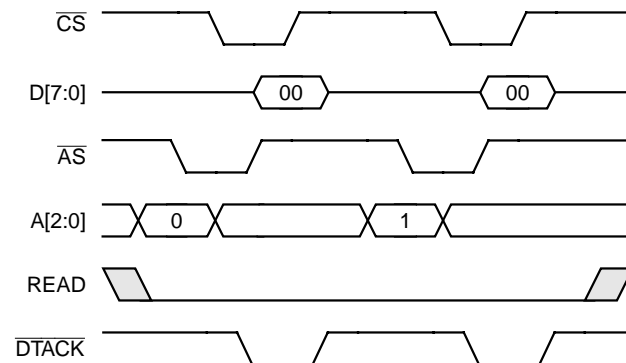
- Step 1. Issue a hard reset to the chip (Figure 3.2). Wait for t_{WK} , 280 OCLK cycles, before the next step.

Figure 3.2
Issue a Hard Reset



- Step 2. Set APR0 and APR1 to zero by writing a zero to addresses 0 and 1. (See Figure 3.3).

Figure 3.3
Initialize APR0 and APR1 to Zero

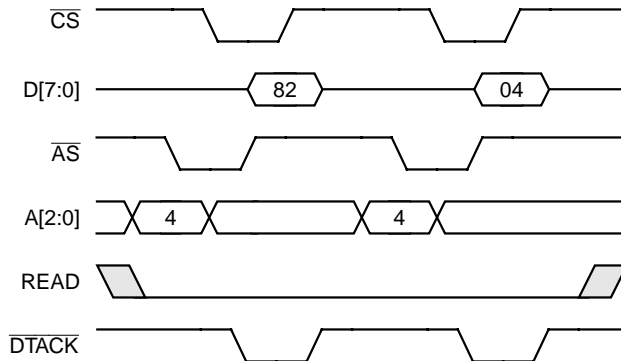


- Step 3. Write to the Configuration registers in Group 4. Start from location zero, and let the auto-increment mechanism advance to the next location with every low-to-high transition of \overline{CS} .

Because the APR registers were both initialized to zero, the first location written is zero, the second location will be one, and so on.

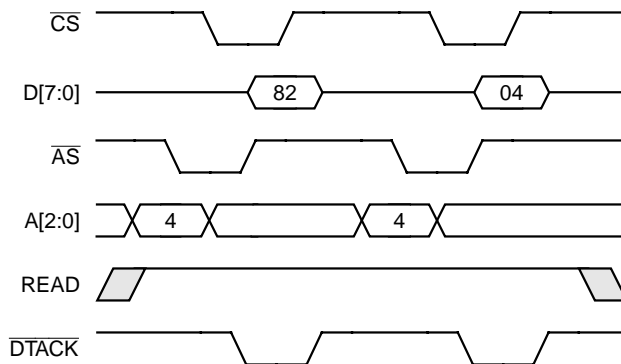
Figure 3.4 and Figure 3.5 present the first two write operations out of the 37 required operations described above.

Figure 3.4
Write Locations 0
and 1 in Group 4



Step 4. You can also choose to read back the L64704's configuration. This is demonstrated in Figure 3.5. You can set APR0 and APR1 to zero, as discussed in Step 2 and step through the configuration locations. The $READ$ signal is asserted, and the auto-increment mechanism selects location 0, then location 1, etc.

Figure 3.5
Read Back
Group 4



Data is valid for a period $t_{DEL D}$ after \overline{CS} goes low.

3.1.2 Programming Using the Serial Interface

Setting the HOST_MODE pin LOW during reset places the L64704 in Serial Host Interface mode. When the L64704 is addressed using the serial interface, it must first be programmed with a 7-bit slave address before any other read or write cycles. [Appendix A, “Programming the L64704 Using the Serial Bus Protocol,”](#) contains a detailed description of the protocol used when programming the L64704 in Serial Host Interface mode.

3.2 Reset and How It Affects Registers

There are three separate resets available on the L64704; the hardware RESET pin, the DEMOD_RST register bit and the FEC_RST register bit (Group 4, APR 36). Each affects the registers differently:

- ◆ Toggling the hardware RESET pin resets all of the Group 2 and Group 3 registers. Registers in Group 4 are unaffected.
- ◆ Setting the DEMOD_RST bit in the External Output Control Bits and Reset Register (Group 4, APR 36) affects only the bits in Group 3 registers that are directly concerned with the demodulator circuitry.
- ◆ Setting the FEC_RST bit in the External Output Control Bits and Reset Register (Group 4, APR 36) resets the System Mode/Status registers (Group 2) and any bits in Group 3 registers that are directly concerned with the demodulator circuitry.

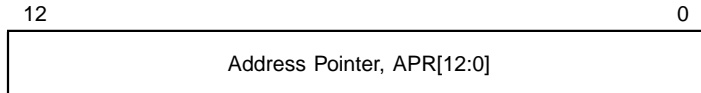
Registers in Group 4 are unaffected by any of these reset operations. Group 4 registers appear random immediately after power-up, and retain their last known value after any of the three reset operations listed above.

The following steps should be followed when resetting the L64704:

- ◆ Issue an active HIGH reset pulse to the RESET pin.
- ◆ Program the Configuration (Group 4) registers to their proper values.
- ◆ Issue a soft reset by setting the DEMOD_RST bit and the FEC_RST bits to 1 (Group 4, APR 36). These bits are self-resetting, and do not have to be cleared.
- ◆ Wait the amount specified by the parameter t_{WK} (see [Figure 8.4](#)).
- ◆ Start the L64704.

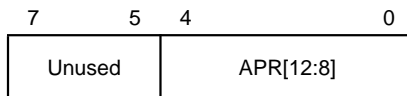
3.3
Group 0, 1
Address Pointer
Register

The Address Pointer Register (APR) is a 13-bit R/W register that points to the registers in Groups 2, 3, and 4. It is accessed when $A[2:0] = 000_2$ and 001_2 . Before accessing a register location from Group 2, 3, or 4, you must initialize the APR with the address of the first register entry that you are going to read or write. The APR automatically increments after reading or writing a byte within a Group 2, 3, or 4 register ($A[2:0] = 010_2$, 011_2 or 100_2).

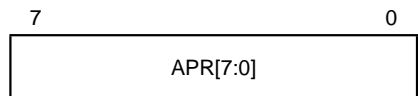


Two consecutive writes are required to load the complete APR. The first write is to Group 0 to load the eight LSBs, the second to Group 1 to load the five MSBs. The APR can be read as well as written.

Group 1, Data Bus D[7:0]



Group 0, Data Bus D[7:0]



The unused bits in these registers are reserved for LSI internal test procedures and future expansion and should always be set to zero.

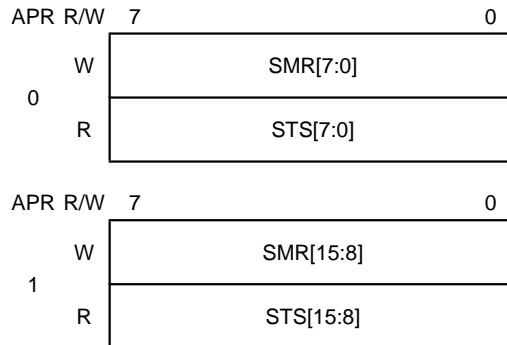
To access a Group 3 or 4 register:

- ◆ Place the address of the lower byte of the register that you need to address into the APR.
- ◆ Read or write the lower byte of the register using the Group 3 register address (0x011) or Group 4 register address (0x100).
- ◆ If the register is a 16-bit register, just perform another read or write to the group register address to access the second byte. The APR increments automatically.

When you are through, the APR will automatically point to the next register in the group.

3.4 Group 2 Registers

Group 2 contains two 16-bit registers; the System Mode Register and the System Status Register. The System Mode Register is accessed by writing the Group 2 address, and the System Status Register is accessed by reading the Group 2 address. Because the L64704 has an 8-bit architecture, each 16-bit register is accessed as two 8-bit registers:



The microcontroller accesses these registers by setting $A[2:0] = 010_2$. It can access these registers at any point during Satellite Decoder operation without interrupting the internal processing unit.

Note: The Phase-Locked Loop must be locked for the status signals to be valid.

3.4.1 System Mode Register (SMR)

The 16-bit System Mode Register (SMR) is a write-only register that allows the external microcontroller to control the L64704. Bits [15:8] of the register enable interrupts for the Demodulator and bits [7:0] of the register enable interrupts for the FEC module.

Because the SMR is arranged as two 8-bit registers, the microcontroller must perform two consecutive writes to the register address. The lower eight bits of the APR must be set to 0x00 before accessing the SMR. The eight LSBs of the SMR are accessed first. The auto-increment mechanism toggles the Address Pointer Register after the first access so that the next write goes to the MSB. If you only want to write the upper byte, you can set APR = 0x01 before the write operation.

The following register diagram shows the bit organization of SMR[15:8]. Descriptions of the fields follow the register diagram. The L64704 sets all the bits in SMR[15:8] to zero after a software or a hardware reset.

APR	D15	D14	D13	D12	D11	D10	D9	D8
1	FS_UL_IE	FS_LL_IE	CF_LLK_IE	CF_LK_IE	CP_LLK_IE	CP_LK_IE	AFC_LLK_IE	AFC_LK_IE

FS_UL_IE Freq. Sweep Upper Limit Reached Interrupt Enable 8
 The microcontroller sets FS_UL_IE to enable an interrupt when the Frequency Sweep has reached its upper limit. The L64704 always sets the FS_UL bit in STS[15:8] when this condition occurs.

FS_UL_IE	Definition
0	Disable Interrupt for Frequency Sweep Upper Limit Reached
1	Enable Interrupt for Frequency Sweep Upper Limit Reached Detect

FS_LL_IE Freq. Sweep Lower Limit Reached Interrupt Enable 9
 The microcontroller sets FS_LL_IE to enable an interrupt when the Frequency Sweep has reached its lower limit. The L64704 always sets the FS_LL bit in STS[15:8] when this condition occurs.

FS_LL_IE	Definition
0	Disable Interrupt for Frequency Sweep Lower Limit Reached Detect
1	Enable Interrupt for Frequency Sweep Lower Limit Reached Detect

CF_LLK_IE Carrier Freq. Lock Lost Detect Interrupt Enable 10
 The microcontroller sets CF_LLK_IE to enable an interrupt when Carrier Frequency Lock Loss is detected (CAR_LCF=0). The L64704 always sets the CF_LLK bit in STS[15:8] when this condition occurs.

CF_LLK_IE	Definition
0	Disable Interrupt for Carrier Frequency Lock Loss Detect
1	Enable Interrupt for Carrier Frequency Lock Loss Detect

CF_LK_IE Carrier Frequency Lock Detect Interrupt Enable 11
 The microcontroller sets CF_LK_IE to enable an interrupt when Carrier Frequency Lock is detected (CAR_LCF=1). The L64704 sets the CF_LK bit in STS[15:8] when this condition occurs.

CF_LK_IE	Definition
0	Disable Carrier Frequency Lock Detect Interrupt
1	Enable Carrier Frequency Lock Detect Interrupt

CP_LLK_IE Carrier Phase Lock Lost Detect Interrupt Enable 12
 The microcontroller sets CP_LLK_IE to enable an interrupt when Carrier Phase Lock Loss is detected (CAR_LC = 0). The L64704 always sets the CP_LLK bit in STS[15:8] when this condition occurs.

CP_LLK_IE	Definition
0	Disable Interrupt for Carrier Phase Lock Loss Detect
1	Enable Interrupt for Carrier Phase Lock Loss Detect

CP_LK_IE Carrier Phase Lock Detect Interrupt Enable 13
 The microcontroller sets CP_LK_IE to enable an interrupt when Carrier Phase Lock is detected (CAR_LC = 1). The L64704 always sets the CP_LK bit in STS[15:8] when this condition occurs.

CP_LK_IE	Definition
0	Disable Interrupt for Carrier Phase Lock Detect
1	Enable Interrupt for Carrier Phase Lock Detect

AFC_LLK_IE Clock AFC Lock Lost Detect Interrupt Enable 14
 The microcontroller sets AFC_LLK_IE to enable an interrupt when Automatic Frequency Controller Lock Loss is detected. The L64704 always sets the AFC_LLK bit in STS[15:8] when this condition occurs.

AFC_LLK_IE	Definition
0	Disable Interrupt for AFC Lock Lost Detect
1	Enable Interrupt for AFC Lock Lost Detect

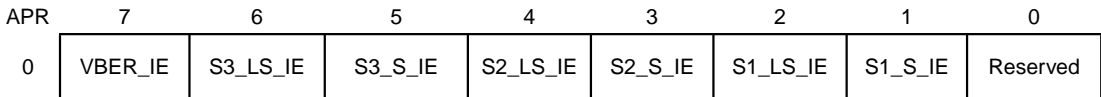
AFC_LK_IE Clock AFC Lock Detect Interrupt Enable 15

The microcontroller sets AFC_LK_IE to enable an interrupt when Automatic Frequency Controller Lock is detected. The L64704 always sets the AFC_LK bit in STS[15:8] when this condition occurs.

AFC_LK_IE Definition

0	Disable Interrupt for AFC Lock Detect
1	Enable Interrupt for AFC Lock Detect

This register diagram shows the bit organization of SMR[7:0]. Descriptions of the fields follow the register diagram. The L64704 clears all bits in the SMR to zero after a software or hardware reset.

**VBER_IE Viterbi Bit Error Rate Monitor Interrupt Enable 7**

The microcontroller sets VBER_IE to enable an interrupt when the Viterbi decoder reaches the period specified by VMDC2 (the period over which the Viterbi bit errors are counted). The L64704 always sets the VBER bit in STS[7:0] when this condition occurs.

VBER_IE Definition

0	Disable Interrupt for Viterbi BER Count
1	Enable Interrupt for Viterbi BER Count

S3_LS_IE Stage 3 Loss of Synchronization Interrupt Enable 6

The microcontroller sets S3_LS_IE to enable an interrupt when Descrambler synchronization is lost.

S3_LS_IE Definition

0	Disable Interrupt for Stage 3 Loss of Synchronization
1	Enable Interrupt for Stage 3 Loss of Synchronization

S3_S_IE **Stage 3 Synchronization Interrupt Enable** **5**
 The microcontroller sets S3_S_IE to enable an interrupt when Descrambler synchronization is established.

S3_S_IE	Definition
0	Disable Interrupt for Stage 3 Synchronization
1	Enable Interrupt for Stage 3 Synchronization

S2_LS_IE **Stage 2 Loss of Synchronization Interrupt Enable** **4**
 The microcontroller sets S2_LS_IE to enable an interrupt when Deinterleaver/Reed-Solomon Decoder synchronization is lost.

S2_LS_IE	Definition
0	Disable Interrupt for Stage 2 Loss of Synchronization
1	Enable Interrupt for Stage 2 Loss of Synchronization

S2_S_IE **Stage 2 Synchronization Interrupt Enable** **3**
 The microcontroller sets S2_S_IE to enable an interrupt when Deinterleaver/Reed-Solomon Decoder synchronization is established.

S2_S_IE	Definition
0	Disable Stage 2 Synchronization Interrupt
1	Enable Stage 2 Synchronization Interrupt

S1_LS_IE **Stage 1 Loss of Synchronization Interrupt Enable** **2**
 The microcontroller sets S1_LS_IE to enable an interrupt when Viterbi Decoder synchronization is lost.

S1_LS_IE	Definition
0	Disable Stage 1 Loss of Synchronization Interrupt
1	Enable Stage 1 Loss of Synchronization Interrupt

S1_S_IE **Stage 1 Synchronization Interrupt Enable** **1**
 The microcontroller sets S1_S_IE to enable an interrupt when Viterbi Decoder synchronization is established.

S1_S_IE	Definition
0	Disable Stage 1 Synchronization Interrupt
1	Enable Stage 1 Synchronization Interrupt

Reserved **Reserved Bit** **0**
 This bit is reserved for LSI Logic internal use only. You should always set this bit to 0.

3.4.2
System Status
Register (STS)

The STS Register is a read-only register that provides the external microcontroller access to status information about the L64704. It provides information about what event caused the generation of an internal interrupt condition. The interrupt status bits are set regardless of the enable interrupt bits in the SMR Register. The internal status is updated every L64704 OCLK. When the microcontroller reads the status, the current information is buffered in a special purpose 16-bit STS buffer that locks the STS value until the end of the microcontroller read operation.

Two consecutive read operations must be done to the same address to get both bytes of the STS. The eight MSBs are the interrupts related to the Demodulation function of the L64704, and the eight LSBs are the interrupts related to the Forward Error Correction function of the L64704.

The status bits are reset after a hardware reset. They are also reset each time that the register byte is read; when you read the eight LSBs, the eight LSB interrupts are cleared, and when you read the eight MSBs, the eight MSB interrupts are cleared. The register diagram below shows a detailed description of the STS[15:8] register bits:

APR	D15	D14	D13	D12	D11	D10	D9	D8
1	FS_UL	FS_LL	CF_LLK	CF_LK	CP_LLK	CP_LK	AFC_LLK	AFC_LK

FS_UL **Frequency Sweep Upper Limit Reached** **0**
 The L64704 sets this bit when the upper limit of the Frequency Sweep is reached.

FS_UL	Definition
0	Frequency Sweep Status Unchanged
1	Frequency Sweep Upper Limit Reached

FS_LL **Frequency Sweep Lower Limit Reached** **1**
 The L64704 sets this bit when the lower limit of the Frequency Sweep is reached.

FS_LL	Definition
0	Frequency Sweep Status Unchanged
1	Frequency Sweep Lower Limit Reached

CF_LLK **Carrier Frequency Lock Lost** **2**
 The L64704 sets this bit when Carrier Frequency Lock is lost.

CF_LLK	Definition
0	Carrier Frequency Lock Status Unchanged
1	Carrier Frequency Lock Lost

CF_LK **Carrier Frequency Lock Established** **3**
 The L64704 sets this bit when Carrier Frequency Lock is established.

CF_LK	Definition
0	Carrier Frequency Lock Status Unchanged
1	Carrier Frequency Lock Established

CP_LLK **Carrier Phase Lock Lost** **4**
 The L64704 sets this bit when Carrier Phase Lock is lost.

CP_LLK	Definition
0	Carrier Phase Lock Status Unchanged
1	Carrier Phase Lock Lost

CP_LK **Carrier Phase Lock Established** **5**
 The L64704 sets this bit when Carrier Phase Lock is established.

CP_LK	Definition
0	Carrier Phase Lock Status Unchanged
1	Carrier Phase Lock Established

AFC_LLK **Clock AFC Lock Lost** **14**
 The L64704 sets this bit when Clock AFC Lock is lost.

AFC_LLK	Definition
0	Clock AFC Lock Status Unchanged
1	Clock AFC Lock Lost

AFC_LK **Clock AFC Lock Established** **15**
 The L64704 sets this bit when Clock AFC Lock is established.

AFC_LK	Definition
0	Clock AFC Lock Status Unchanged
1	Clock AFC Lock Established

The register diagram below shows a detailed description of the STS[7:0] register bits.

APR	7	6	5	4	3	2	1	0
0	VBER	S3_LS	S3_S	S2_LS	S2_S	S1_LS	S1_S	Reserved

VBER **Viterbi Bit Error Rate Flag** **7**

The L64704 sets VBER when the period specified by VMDC2 (Group 4, APRs 5, 6, and 7) is reached. It also generates an interrupt if the VBER_IE bit in the SMR is set. The L64704 clears VBER to zero after a reset or a Group 2 (STS) read.

VBER	Definition
0	VMDC2 Period not Reached
1	VMDC2 Period Reached

S3_LS **Stage 3 Loss of Synchronization Flag** **6**

The L64704 sets S3_LS when the Descrambler synchronization module determines that synchronization is lost. It also generates an interrupt if the S3_LS_IE bit is set in the SMR. The L64704 clears S3_LS to zero after a reset or a Group 2 (STS) read.

S3_LS	Definition
0	Stage 3 Synchronization Status Unchanged
1	Loss of Stage 3 Synchronization Detected

S3_S **Stage 3 Synchronization Flag** **5**

The L64704 sets S3_S when the Descrambler synchronization module acquires synchronization. It also generates an interrupt if the S3_S_IE bit is set in the SMR. The L64704 clears S3_S to zero after a reset or a Group 2 (STS) read.

S3_S	Definition
0	Stage 3 Synchronization Status Unchanged
1	Stage 3 Synchronization Acquired

S2_LS **Stage 2 Loss of Synchronization Flag** **4**

The L64704 sets S2_LS when the Deinterleaver/Reed-Solomon Decoder synchronization module determines that synchronization is lost. It also generates an interrupt

if the S2_LS_IE bit is set in the SMR. The L64704 clears S2_LS to zero after a reset or a Group 2 (STS) read.

S2_LS	Definition
0	Stage 2 Synchronization Status Unchanged
1	Loss of Stage 2 Synchronization Detected

S2_S **Stage 2 Synchronization Flag** **3**
 The L64704 sets S2_S when the Deinterleaver/Reed-Solomon Decoder synchronization module acquires synchronization. It also generates an interrupt if the S2_S_IE bit is set in the SMR. The L64704 clears S2_S to zero after a reset or a Group 2 (STS) read.

S2_S	Definition
0	Stage 2 Synchronization Status Unchanged
1	Stage 2 Synchronization Acquired

S1_LS **Stage 1 Loss of Synchronization Flag** **2**
 The L64704 sets S1_LS when the Viterbi Decoder synchronization module determines that synchronization is lost. It also generates an interrupt if the S1_LS_IE bit is set in the SMR. The L64704 clears S1_LS to zero after a reset or a Group 2 (STS) read.

S1_LS	Definition
0	Stage 1 Synchronization Status Unchanged
1	Loss of Stage 1 Synchronization Detected

S1_S **Stage 1 Synchronization Flag** **1**
 The L64704 sets S1_S when the Viterbi Decoder synchronization module has acquired synchronization. It also generates an interrupt if the S1_S_IE bit is set in the SMR. The L64704 clears S1_S to zero after a reset or a Group 2 (STS) read.

S1_S	Definition
0	Stage 1 Synchronization Status Unchanged
1	Stage 1 Synchronization Acquired

Reserved **Reserved Bit** **0**
 This bit is reserved for LSI Logic internal use only. Reading this bit will give unpredictable results.

3.5 Group 3 Registers

Group 3 consists of a number of internal status registers that are used for diagnostics and performance evaluation purposes. The registers are updated every OCLK cycle. When the microcontroller reads the register, the current information is buffered in a special purpose buffer that stores the value of the respective register until the end of the read operation. The L64704 clears all the bits in the Group 3 registers to zero after a software or a hardware reset.

Table 3.3 shows the addresses and fields of the Group 3 registers.

Table 3.3
Group 3 Register Map

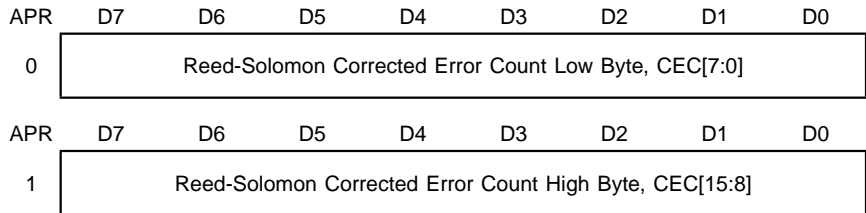
APR	D7	D6	D5	D4	D3	D2	D1	D0
0	Reed-Solomon Corrected Error Count Low Byte, CEC[7:0]							
1	Reed-Solomon Corrected Error Count High Byte, CEC[15:8]							
2	Reed-Solomon Uncorrected Error Count Low Byte, UEC[7:0]							
3	Reed-Solomon Uncorrected Error Count High Byte, UEC[15:0]							
4	Viterbi Bit Error Rate Count Low Byte, VBERC[7:0]							
5	Viterbi Bit Error Rate Count High Byte, VBERC[15:8]							
6	Demod_ SNR	XCTR_IN	Measured Carrier VCO Frequency, CAR_VCOF[13:8]					
7	Measured Carrier VCO Frequency, CAR_VCOF[7:0]							
8	AGC Loop Voltage Meter, PWR_LVL[7:0]							
9	Reserved		CAR_LCF	CAR_LC	CLK_LCF	S3	S2	S1
10	Reserved		RI Readback, RI[5:0]					
11	Reserved		RQ Readback, RQ[5:0]					

3.5.1
Group 3,
APR 0, 1
RS Corrected
Error Count

When read, this register presents a count of corrected errors since it was last reset. When written, the register is reset to zero. CEC is 16-bits long, where the LSB is found on APR 0, bit 0, and the MSB on APR 1, bit 7. The CEC counter is incremented each time that a byte is corrected, independent of the number of bit errors that are encountered in the byte. It is not incremented when a block is flagged as uncorrectable. The CEC counter will wrap around when it reaches its maximum count.

Read/Write: R/W

Reset Value: 0x0000

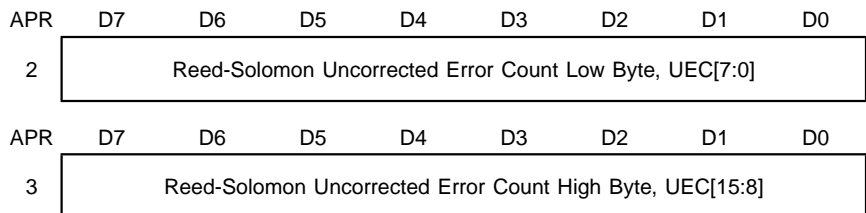


3.5.2
Group 3,
APR 2, 3
RS Uncorrected
Error Count

When read, this register presents a count of the uncorrected code words since it was last reset. When written, the register is set to zero. UEC is 16 bits long, where the LSB is found on APR 2, bit 0, and the MSB on APR 3, bit 7. The UEC count stops when it reaches its maximum count (65535), and the counter is reset each time that it is read.

Read/Write: R/W

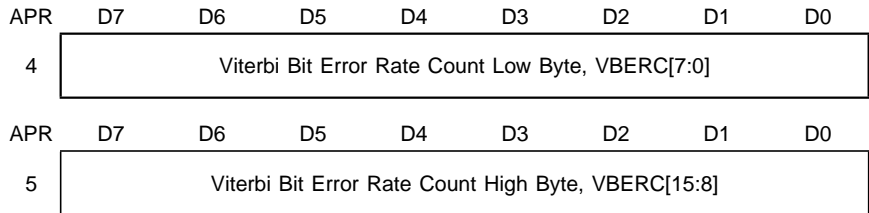
Reset Value: 0x0000



3.5.3
Group 3,
APR 4, 5
Viterbi Bit Error
Count

When read, this register presents a count of the number of Viterbi decoder bit errors found during the time period specified by VMDC2 (Group 4, APR [5:5]). VBERC is 16-bits long, where the LSB is found on APR 4, bit 0, and the MSB on APR 5, bit 7. The actual number of errors is equal to four times VBERC. VBERC is updated each time that a Viterbi error is encountered, and it is reset at the beginning of each VMDC2 period.

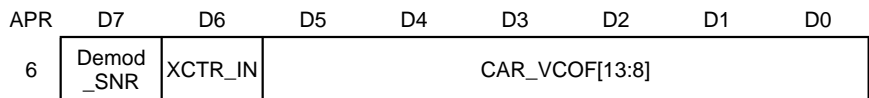
Read/Write: R **Reset Value: 0x0000**



3.5.4
Group 3,
APR 6
Control Input
and SNR

This register contains the Control Input bit(s), the Demodulator SNR bit, and the five upper bits of the Measured VCO Frequency. The Control Input bit(s) and the Demodulator SNR bit are discussed here, the Measured VCO Frequency field CAR_VCOF[13:8], is discussed in the next section.

Read/Write: R/W **Reset Value: 0x0000**



Demod_SNR Demodulator Signal to Noise Ratio **7**

When read, this bit gives an indication of the SNR. When the SNR is bad, this bit is 0; when it is good, this bit is 1. A “bad” SNR is above the threshold; a “good” SNR is below the threshold. See [Section 5.6.2.1, “Phase Error Estimator,”](#) and [Figure 5.7](#) for details.

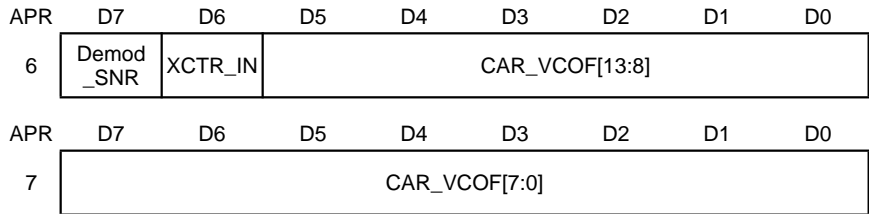
XCTR_IN External Control Input Bit **6**

When read, this bit shows the logic level applied to the External Control Input (XCTR_IN) pin.

3.5.5
Group 3,
APR 6, 7
Measured VCO
Frequency

The L64704 puts the result of the VCO frequency measurement into this 16-bit register. Both the upper and lower nibbles must be read before the L64704 releases this register for a new value. See [Section 5.6.1.2, “Carrier VCO Frequency Measurement,”](#) for details on how the L64704 computes this value.

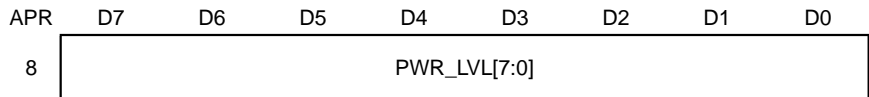
Read/Write: R **Reset Value: 0x0000**



3.5.6
Group 3,
APR 8
AGC Loop
Voltage Meter

The L64704 stores the AGC loop control voltage in this register. See [Section 5.7.3, “Power Level,”](#) for an equation that relates V_{AGC} and PWR_LVL.

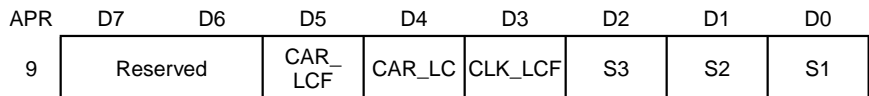
Read/Write: R **Reset Value: 0x00**



3.5.7
Group 3,
APR 9
Carrier and FEC
Synchronization
Status

This register contains the Carrier Loop and FEC pipeline synchronization status bits.

Read/Write: R **Reset Value: 0x00**



Reserved **Reserved Bits [7:6]**
 These bits are reserved for LSI Logic internal use only. When read, they will return an indeterminate value.

CAR_LCF **Carrier Frequency Lock Flag** **5**
The L64704 sets CAR_LCF to 1 to indicate that the carrier frequency lock detector is in lock.

CAR_LCF	Definition
0	Carrier Frequency Lock Detector Out of Lock
1	Carrier Frequency Lock Detector Locked

CAR_LC **Carrier Phase Lock Flag** **4**
The L64704 sets CAR_LC to 1 to indicate that the carrier phase lock detector is locked.

CAR_LC	Definition
0	Carrier Phase Lock Detector Out of Lock
1	Carrier Phase Lock Detector Locked

CLK_LCF **Clock Frequency Lock Flag** **3**
The L64704 sets CLK_LCF to 1 to indicate that the clock generated by the AFC control is within pull-in range of the clock recovery loop.

CLK_LCF	Definition
0	Clock Frequency Out of Lock
1	Clock Frequency Locked

S3 **Stage 3 Synchronization Flag** **2**
The L64704 sets S3 to 1 when the Descrambler synchronization module is in synchronization. When this bit is 0, the Descrambler module is not synchronized.

S3	Definition
0	Descrambler Out of Synchronization
1	Descrambler In Synchronization

S2 **Stage 2 Synchronization Flag** **1**
 The L64704 sets S2 to 1 when the Deinterleaver/Reed-Solomon Decoder synchronization module is in synchronization. When this bit is 0, the Deinterleaver/Reed-Solomon Decoder is not synchronized.

S2	Definition
0	Deinterleaver/Reed-Solomon Decoder Out of Synchronization
1	Deinterleaver/Reed-Solomon Decoder In Synchronization

S1 **Stage 1 Synchronization Flag** **0**
 The L64704 sets S1 to 1 when the Viterbi Decoder synchronization module is in synchronization. When this bit is 0, the Viterbi Decoder is not synchronized.

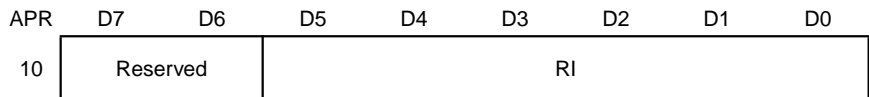
S1	Definition
0	Viterbi Decoder Out of Synchronization
1	Viterbi Decoder In Synchronization

3.5.8
Group 3,
APR 10
RI Readback

This register displays the value on the RI[5:0] input bus. Group 3, RI values are only correct when the PLL is set such that ICLK = OCLK.

Read/Write: R

Reset Value: 0x00



Reserved **Reserved Bits** **[7:6]**
 These bits are reserved for LSI Logic internal use only. When read, they will return an indeterminate value.

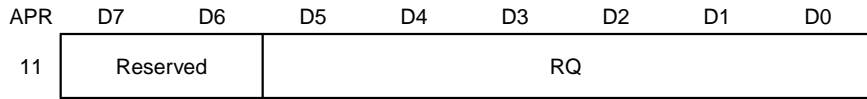
RI **RI Readback** **[5:0]**
 This register displays the value on the RI[5:0] input bus. (Note that OCLK needs to be running for this feature to operate properly).

**3.5.9
Group 3,
APR 11
RQ Readback**

This register displays the value on the RQ[5:0] input bus. Group 3, RQ values are only correct when the PLL is set such that ICLK = OCLK.

Read/Write: R

Reset Value: 0x00



Reserved **Reserved Bits** **[7:6]**

These bits are reserved for LSI Logic internal use only. When read, they will return an indeterminate value.

RQ **RQ Readback** **[5:0]**

This register displays the value on the RQ[5:0] input bus. (Note that OCLK needs to be running for this feature to operate properly).

**3.6
Group 4
Registers**

Most Group 4 registers are 8 bits wide while some registers are wider (up to 24 bits). All accesses are done in 8-bit widths. The Address Pointer Register (APR) is used to access these registers as described in Section 3.3, “[Group 0, 1 Address Pointer Register](#).”

Group 4 registers are not affected by a reset. Group 4 registers appear random immediately after power-up, and retain their last known value after any of the three reset operations as shown in 3.2, “[Reset and How It Affects Registers](#).” Table 3.4 shows the addresses and fields of the Group 4 registers.

Table 3.4
Group 4 Register Map

APR[5:0]	D7	D6	D5	D4	D3	D2	D1	DO
0	Set to 1	Set to 0	PLL_N[5:0]					
1	Set to 0	Set to 0	PLL_S[5:0]					
2	IMQ	Set to 1	QB	PLL_T[4:0]				
3	Viterbi Code Rate, VCR[2:0]		TEI	SYNC2_MOD	Set to 0	PLL_M[1:0]		
4	Viterbi Max Data Bit Count, VMDC1[7:0]							
5	Viterbi Max Data Bit Count 2, VMDC2[7:0], Low Byte							
6	Viterbi Max Data Bit Count 2, VMDC2[15:8], Middle Byte							
7	Viterbi Max Data Bit Count 2, VMDC2[23:16], High Byte							
8	Viterbi Maximum Bit Error Count, VMBEC[7:0]							
9	Synchronization Word, Sync[7:0]							
10	BER	Reserved					L[1:0]	
11	BF	Set to 0	Sync Status Select, SSS[1:0]		Sync States Acq, SSA [1:0]		Sync States Track, SST[1:0]	
12	BPS[2:0]		Set to 0	OF	Output Selector, OS[2:0]			
13	PLL_RESET							
14	SYNC/ SCLK	Reserved	Set to 0	F_OUT_ HiZ	CLK_LCF_ SUPPRESS	CLK_VC_ SWAP	CLK_DR[1:0]	
15	Set to 0	PCLK_BP	Set to 0	PD	CLK_RP[3:0]			
16	CLK_NF[15:8]							
17	CLK_NF[7:0]							
18	Reserved				CLK_RATIO[2:0]			
19	PWR_REF[7:0]							
20	Reserved				INT_DC	PWR_BW[1:0]		
21	Scale Factor for DEMI, DEMQ, SCALE[7:0]							
22	SNR Estimator Threshold, SNR_THS[7:0]							
23	Carrier Loop DC Offset Compensation, CAR_OFFSET[7:0]							
24	Reserved				Carrier Reference Period, CAR_RP[3:0]			
25	Carrier Loop Filter Gain (P Term), CAR_KP[7:0]							
26	Carrier Loop Filter Gain (D Term), CAR_KD[7:0]							
27	Carrier Lock Detector Threshold, CAR_THSL[7:0]							
28	Carrier Sweep Rate, CAR_SWR[7:0]							
29	Reserved		Carrier Upper Sweep Limit, CAR_USWL[13:8]					
30	Carrier Upper Sweep Limit, CAR_USWL[7:0]							
31	Reserved		Carrier Lower Sweep Limit, CAR_LSWL[13:8]					
32	Carrier Lower Sweep Limit, CAR_LSWL[7:0]							
33	CAR_SWP_ SWAP	CAR_VCO_ SWAP	CAR_VCO 2N/P	CAR_VCO 1N/P	CAR_OUT_S EL	CAR_PED_ SEL	CAR_ OPEN	CAR_SW
34	Set to 0			Reserved				
35	SNR_EST	CON_SEL	Set to 0	FP_LOCK_ LEN	PWRP	Set to 0		I_FORMAT
36	Reserved		External Control Output Bits, XCTR[3:0]				DEMOD_ RST	FEC_ RST

3.6.1
Group 4,
APR 0 PLL
Parameter N

PLL Configuration Parameter N is used to configure the PLL module for clock synthesis.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
0	Set to 1	Set to 0	PLL_N[5:0]					

Set to 1 **Set to 1** **7**
 LSI Logic internal test bit. You must set this bit to 1.

Set to 0 **Set to 0** **6**
 LSI Logic internal test bit. You must set this bit to 0.

PLL_N **PLL Configuration Parameter N** **[5:0]**
 PLL_N[5:0] is one of four parameters (PLL_S, PLL_N, PLL_T, PLL_M) that you must set to configure the PLL module for clock synthesis. For more information see Section 4.4, “PLL Clock Generation.”

3.6.2
Group 4,
APR 1 PLL
Parameter S

PLL Configuration Parameter S is used to configure the PLL module for clock synthesis.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
1	Set to 0		PLL_S[5:0]					

Set to 0 **Set to 0** **[7:6]**
 LSI Logic internal test bit. You must set these bits to 0.

PLL_S **PLL Configuration Parameter S** **[5:0]**
 PLL_S[5:0] is one of 4 parameters (PLL_S, PLL_N, PLL_T, PLL_M) that you must set to configure the PLL module for clock synthesis. For more information see Section 4.4, “PLL Clock Generation.”

**3.6.3
Group 4,
APR 2 PLL
Parameter T,
Demodulator
and Symbol
Select**

PLL Configuration Parameter T is used to configure the PLL module for clock synthesis. This register also contains bits to configure the demodulator and select the symbol format.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
2	IMQ	Set to 1	QB	PLL_T[4:0]				

IMQ **(I, -Q) Symbol Format** **7**
The bit IMQ indicates the format of the incoming symbol stream. In BPSK mode, IMQ must be set to zero.

IMQ	Symbol Format
0	I, Q
1	I, -Q

Set to 1 **Set to 1** **6**
This bit must be set to 1 for proper operation.

QB **QPSK/BPSK Format Select** **5**
Set the QB bit to specify the format of the incoming symbol stream. The QB bit should be set to 0 for systems that input a QPSK symbol pair (I, Q) once per ICLK cycle. The QB bit should be set to 1 for BPSK input (I stream only).

QB	Symbol Stream Format
0	QPSK
1	BPSK

PLL_T **PLL Configuration Parameter T** **[4:0]**
PLL_T[4:0] is one of four parameters (PLL_S, PLL_N, PLL_T, PLL_M) that you must set to configure the PLL module for clock synthesis. For more information see Section 4.4, “PLL Clock Generation.”

**3.6.4
Group 4,
APR 3 PLL
Parameter M,
Transport and
Viterbi Code
Rate Select**

PLL Configuration Parameter M is used to configure the PLL module for clock synthesis. This register also contains bits to set the Viterbi Decoder module code rate and configure the Transport Error Indicator.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
3	Viterbi Code Rate, VCR[2:0]			TEI	SYNC2_ MOD	Set to 0	PLL_M[1:0]	

VCR[2:0] Viterbi Code Rate [7:5]
Set these bits to SELECT the code rate for the Viterbi decoder module on the L64704. The three bits are assigned as follows:

Data Bits

D7 D6 D5 Definition

0	0	0	Rate 1/2
0	0	1	Rate 2/3
0	1	0	Rate 3/4
0	1	1	Rate 5/6
1	0	0	Rate 7/8
1	0	1	Unused
1	1	0	Unused
1	1	1	Unused

TEI Transport Error Indicator Select 4
You set the Transport Error Indicator Select bit to 1 to activate the transport error indicator mechanism. In this mode, the first bit following the synchronization byte in a Transport Packet is forced HIGH whenever the data block was found to be uncorrectable by the Reed-Solomon decoder. Otherwise it remains unchanged. When TEI is set to 0, the transport error indicator will not be set at any time. (See the MPEG-2 System Specification H.222, paragraph 2.4.3.2 Transport Stream Packet Layer.) Using the TEI feature allows a simpler interface to the LSI Logic L64007 Transport Demultiplexer. For more information, see LSI Logic *L64007 MPEG-2, DVB, and TSAT Transport Demultiplexer Technical Manual*.

SYNC2_MOD	Sync 2 Modified	3
	This bit selects an alternate method of acquiring Sync 2. It should be set to 1 for normal operation.	
Set to 0	Set to 0	2
	This bit must be set to 0 for proper operation.	
PLL_M	VCO Frequency Range for PLL Module	[1:0]
	PLL_M is one of four parameters (PLL_S, PLL_N, PLL_T, PLL_M) that you must set to configure the PLL module for clock synthesis. For more information see Section 4.4, “PLL Clock Generation.” Set PLL_M[1:0] to tell the L64704 the frequency range of the VCO.	

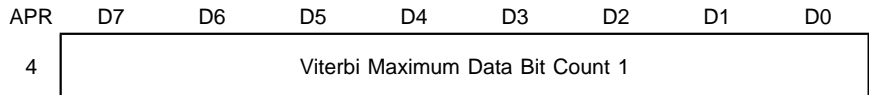
Data Bits

D1	D0	VCO Range
0	0	40 - 50 MHz
0	1	50 - 60 MHz
1	0	60 - 70 MHz
1	1	70 - 80 MHz

3.6.5
Group 4,
APR 4
Viterbi Max Data
Bit Count 1

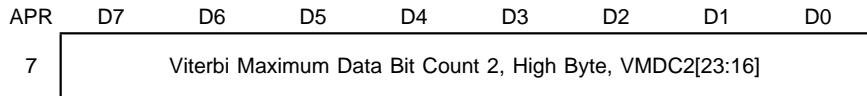
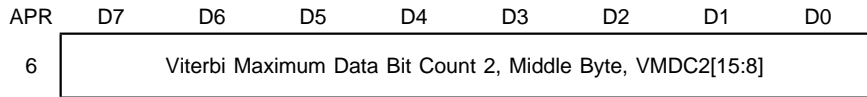
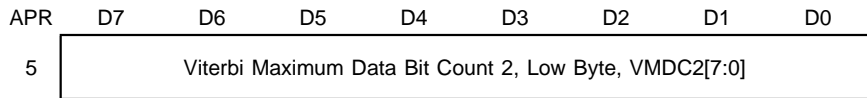
VMDC1 specifies the number of valid symbols, divided by 256, over which the number of Viterbi decoded symbol errors are counted for synchronization. For example, a value of VMDC1[7:0] = 0b0000001 specifies 512 data bits. For more information see Section 7.1.4, “Viterbi Bit Error Rate Monitor.”

Read/Write: R/W



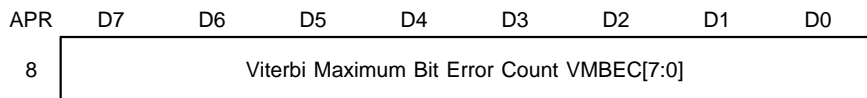
3.6.6
Group 4,
APR 5, 6, 7
Viterbi Max Data
Bit Count 2

VMDC2 specifies the number of valid symbols, divided by 4, over which the number of symbol errors in the Viterbi output data stream are counted, after synchronization. The symbol error count is then displayed as VBERC (Group 3, APR 4:5). The value for VMDC2 occupies 24 bits and is arranged as three bytes with APR 5, bit 0 being the least significant bit and APR 7, bit 7 being the most significant bit. For example, a value of VMDC2[23:0] = 0x0000F0 specifies 960 data bits. For more information see Section 7.1.4, “Viterbi Bit Error Rate Monitor.”

Read/Write: R/W

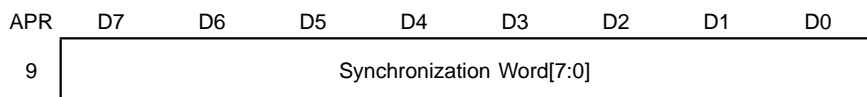
3.6.7
Group 4,
APR 8
Viterbi
Maximum Bit
Error Count

VMBEC specifies the maximum number of (Viterbi symbol errors/128 + 32) that are allowed to occur within the data period set by VMDC1 (Group 4, APR 4) to achieve Viterbi module synchronization. Whenever the symbol error count from the internal bit error counter exceeds the value VMBEC, the synchronization module concludes that the Viterbi decoder module is out of synchronization and proceeds to adjust the phase of the incoming symbol stream until synchronization is reached. For example, a value of VMBEC[7:0] = 0b00000011 specifies 416 errors. For more information see [Equation 7.1](#) in Section 7.1.4, “Viterbi Bit Error Rate Monitor.”

Read/Write: R/W

3.6.8
Group 4,
APR 9
Synchronization
Word

This register contains the synchronization word used by the synchronization module in stages two and three. Within this byte, the MSB is oldest chronologically, and the LSB the newest.

Read/Write: R/W

**3.6.9
Group 4,
APR 10
BER Monitor
and
Mismatching
Bits in Sync 2
Tracking Mode**

This register is used to set the maximum number of mismatching bits allowed to declare a match when comparing the data stream to the reference synchronization word during the tracking phase in the second synchronization stage.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
10	Set to 0	Reserved					L[1:0]	

Set to 0 **Set to 0** **7**
This is an internal test bit and should be set to 0 for normal operation.

Reserved **Reserved Bits** **[6:2]**
These bits are reserved for LSI Logic internal use only. Reserved bits should always be set to 0, and will produce random results when read.

L[1:0] **Mismatching Bits, Tracking Mode, Sync 2** **[1:0]**
This field is used to set the maximum number of mismatching bits allowed to declare a match when comparing eight bits in the data stream to the reference synchronization word during tracking phase in the second synchronization stage. L can be configured from 0 to 2. A higher value of L results in a smaller probability of loss of lock due to random noise, a lower value in a higher probability of loss.

Data Bits		Number of Mismatching Bits
D1	D0	
0	0	0
0	1	1
1	0	2
1	1	Illegal Value

3.6.10
Group 4,
APR 11
Synchronization
States and
BCLKOUT
Format

This register is used to select which algorithms will be used in the synchronization modules, and which module's synchronization status will be shown on the SYNC output pin. It also selects the frequency of the clock that will be output on the BCLKOUT pin.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
11	BF	Set to 0	SSS[1:0]		SSA[1:0]		SST[1:0]	

BF **BCLKOUT Format** **7**

When you set this bit to 1, the BCLKOUT pin outputs a continuous clock waveform with a 50% duty cycle at 1/8 the OCLK frequency. It is typically used by a downstream device that runs on a byte-clock rather than on a bit clock. The DVALIDOUT pin needs to be observed to identify valid data bytes. When you set this bit to 0, the BCLKOUT produces a rising edge for every valid data bit on the CO0 output pin (Serial Output Channel mode). The downstream device can use BCLKOUT as a data latching strobe without the need to inspect DVALIDOUT.

Data Bits	BCLKOUT	Operating Mode
D7	Function:	
1	Continuous Clock	Serial Output Channel
0	Data Strobe	Parallel Output Channel

Set to 0 **Set to 0** **6**
 You should set this bit LOW for proper operation.

SSS[1:0] **Synchronization Status Select** **[5:4]**
 You can observe the synchronization status of one of the three synchronization modules on the SYNC output pin: Viterbi decoder synchronization, Deinterleaver/Reed-Solomon decoder synchronization, and Descrambler synchronization. You program the SSS field to determine

which one of these three synchronization status bits will be propagated to the SYNC pin.

Data Bits		SYNC Pin Connected to
D5	D4	
0	0	Viterbi Decoder Synchronization
0	1	DI/RS Decoder Synchronization
1	0	Descrambler Synchronization

SSA[1:0] Synchronization States, Acquisition Mode [3:2]

The second synchronization module (after the Viterbi Decoder, before the Deinterleaver module) allows three different state diagrams to be used in the acquisition phase. The number of properly identified synchronization words that will cause “in-synchronization” to be declared can be configured from 3 to 6. For more information see Section 6.3, “[Reed-Solomon Deinterleaver Synchronization](#).”

Data Bits		Number of Sync Words Found to Acquire
D3	D2	
0	0	3
0	1	4
1	0	5
1	1	6

SST[1:0] Synchronization Status, Tracking Mode [1:0]

The second synchronization module (after the Viterbi decoder and before the Deinterleaver module) allows two, three, four, or five undetected synchronization words before the L64704 declares a loss of sync. For more information see Section 6.3, “[Reed-Solomon Deinterleaver Synchronization](#).”

Data Bits		Number of Missed Sync Words to Loss of Lock
D1	D0	
0	0	2
0	1	3
1	0	4
1	1	5

3.6.11
Group 4,
APR 12
Output Control

This register is used to configure the Channel output data path.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
12	BPS[2:0]			Set to 0	OF	OS[2:0]		

BPS[2:0] Symbol Size for Viterbi Bypass Mode [7:5]
 You should set these bits to 0 for proper operation.

Set to 0 Set to 0 4
 You should set this bit to 0 for proper operation.

OF Descrambler Output Format 3
 Writing to this bit sets the descrambler output mode:

D3 Data Bit CO[7:0] Channel Output Mode

0	Serial Channel Output Mode
1	Parallel Channel Output Mode

In Serial Channel Output mode, one bit of decoded data is presented on CO0 every OCLK cycle. In Parallel Channel Output mode, one byte of decoded data is presented on CO[7:0] every eight OCLK cycles.

OS[2:0] Output Selector [2:0]
 The output of several major functional blocks can be observed on the channel output (CO[7:0] in Parallel Channel Output mode, CO0 in Serial Channel Output mode). For a detailed description of the signals observed for the cases below, see Section 4.5, “Data Path Output Configurations.”

Data Bits

D2 D1 D0 Definition

0	0	0	Descrambler Module Output
0	0	1	Descrambler Module Synchronization (Sync 3) Output
0	1	0	RS Decoder Output
0	1	1	Deinterleaver Module Output
1	0	0	Deinterleaver/RS Synchronization (Sync 2) Output
1	0	1	Viterbi Decoder Module Output
1	1	0	Viterbi Synchronization/Decoder Synchronization (Sync 1) Output

Data Bits

D2 D1 D0 Definition

1	1	1	BPSK/QPSK Demodulator Output
---	---	---	------------------------------

3.6.12 Group 4, APR 13 PLL Reset

Writing any value to APR 13 generates an internal reset pulse for the PLL module. The L64704 ignores any data on the D[7:0] bus during a write to this register. You should reset the PLL module before operation.

The PLL Reset register (APR 13) cannot be read.

Read/Write: Write Only

APR	D7	D6	D5	D4	D3	D2	D1	D0
13	PLL_RESET							

3.6.13 Group 4, APR 14 Clock Loop Control 1

The Clock Loop Control 1 register is used to set clock parameters related to the Demodulator module carrier synchronization logic.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
14	SYNC/ SCLK	Reserved	Set to 0	F_OUT_ HiZ	CLK_LCF Suppress	CLK_VCO _SWAP	CLK_DR[1:0]	

SYNC/SCLK SYNC Pin Output Select 7

Use this pin to select the signal that you want to appear on the SYNC pin:

D7	Output	When Used
0	SYNC	Normal Operation
1	SCLK	Low Baud Rate Operations

When this bit is set to 0, the SYNC pin carries the signal selected by the Synchronization Status Select bits SSS[1:0] (Group 4, APR 11). When this bit is set to 1, the SYNC pin carries the symbol clock of the demodulator, SCLK, that is used to clock the external DAC during low baud rate operation. For more information see Section [5.6.2.3, "Low Baud Rate Operation."](#)

Reserved **Reserved Bits** **6**
 These bits are reserved for LSI Logic internal use only. Reserved bits should always be set to 0, and will produce random results when read.

Set to 0 **Set to 0** **5**
 You should set this bit to 0 for proper operation.

F_OUT_HiZ **Functional Outputs 3-stated** **4**
 Set this bit to put the CLK_VCOP/N pins into a high impedance condition.

D4 Definition	
0	Normal
1	Hi-Z

CLK_LCF_Suppress **CLK_LCF_Suppress in Timing Error Detector** **3**
 Set this bit to disable the Automatic Frequency Controller (AFC). For more information see Section 5.5.2, “[Clock Acquisition and Tracking Modes.](#)”

D3 Definition	
0	Normal
1	Suppressed

CLK_VCO_SWAP **CLK Outputs Polarity Swap** **2**
 Program this bit to set the polarity of the clock output pins CLK_VCOP/N. For more information see Section 5.5, “[Channel Clock Recovery.](#)”

D2 Definition	
0	Normal
1	Swapped

CLK_DR[1:0] **Decimation Filter Select** **[1:0]**
 Program the Decimation Filter Select field to set the amount of decimation, and therefore the oversampling ratio. For more information see Section 5.3, “[Decimation Filters.](#)”

D1	D0	Decimation	Oversampling Ratio
0	0	none	2
0	1	1/2	4
1	0	2/3	3
1	1	Illegal	

**3.6.14
Group 4,
APR 15
Clock Loop
Control 2**

The Clock Loop Control 2 register is used to set clock parameters related to the Demodulator module Automatic Frequency Control (AFC) and external phase-locked loop. It also contains the power-down control bit.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
15	Set to 0	PCLK_BP	Set to 0	PD	CLK_RP[3:0]			

Set to 0 **Set to 0** **7**
You should set this bit to 0 for proper operation.

PCLK_BP **PCLK Bypass** **6**
When you set this bit to 0, the PCLK output pin carries the clock signal generated by the internal PLL module. When you set this bit to 1, PCLK presents SCLK at the output and bypasses the internal PLL module. For a block diagram see Section 4.1, “[Data Control and Clocking Schemes.](#)”

Set to 0 **Set to 0** **5**
You should set this bit to 0 for proper operation.

PD **Power-Down** **4**
When you set Power-Down to 1, all modules except the asynchronous microprocessor interface are turned off to reduce power consumption to a minimum. No data processing can occur during Power-Down. When you set Power-Down to 0 all elements operate. You should apply a reset pulse after you change Power-Down from 1 to 0 (wake-up) before you start processing data.

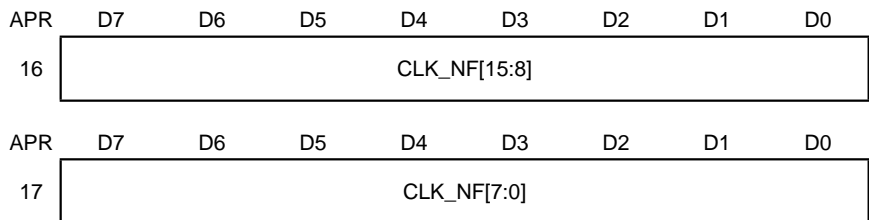
Definition	D4
Normal Operation	0
Device in Power-Down Mode	1

CLK_RP[3:0] Reference Period for Clock AFC [3:0]
 CLK_RP presets the four MSBs of the reference counter. See [Section 5.5.2, “Clock Acquisition and Tracking Modes”](#) for details.

**3.6.15
 Group 4,
 APR 16, 17
 Nominal
 Frequency of
 Clock Input**

A counter in the AFC decrements once each VCO clock edge during the reference period. Set the counter’s initial value using the 16-bit CLK_NF register where bit 7 of APR 16 is the MSB, and bit 0 of APR 17 is the LSB. See [Section 5.5.2, “Clock Acquisition and Tracking Modes”](#) for details.

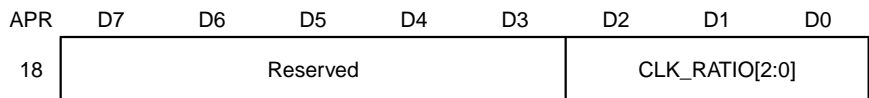
Read/Write: R/W



**3.6.16
 Group 4,
 APR 18
 Clock Ratio**

This register is used to set the input decimation factor for the RI and the RQ inputs.

Read/Write: R/W



Reserved [7:3]
 These bits are reserved for LSI Logic internal use only. Reserved bits should always be set to 0, and will produce random results when read.

CLK_RATIO[2:0] Input Decimation Factor for RI and RQ Inputs [2:0]
 This field sets the input decimation factor for the RI and the RQ inputs. For more information see [Section 5.5.1, “Input Decimation.”](#)

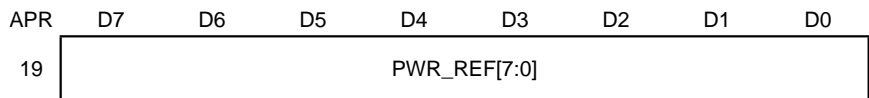
D2	D1	D0	Definition
0	0	0	No Decimation
0	0	1	Input Every Second Sample
0	1	0	Input Every Fourth Sample

D2	D1	D0	Definition
0	1	1	Input Every Eighth Sample
1	0	0	Input Every Sixteenth Sample
1	0	1	Illegal
1	1	0	Illegal
1	1	1	Illegal

3.6.17
Group 4,
APR 19
Power
Reference Level

This register sets the reference power level for the Analog to Digital Convertor. For details on setting this register, see Section 5.7.1, “ADC Range and Power Reference.”

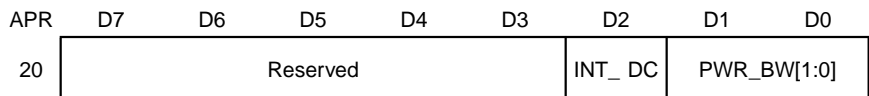
Read/Write: R/W



3.6.18
Group 4,
APR 20
Power
Estimation
Bandwidth and
I/Q DC Offset

This register is used to enable internal DC offset compensation on the I and Q signals and set the power estimation bandwidth.

Read/Write: R/W



Reserved **Reserved** **[7:3]**

These bits are reserved for LSI Logic internal use only. Reserved bits should always be set to 0, and will produce random results when read.

INT_DC **Internal DC Offset Compensation on I and Q** **2**

Set this bit to enable internal DC offset compensation on the I and Q signals.

D2	Definition
0	Disabled
1	Enabled

PWR_BW[1:0] Power Estimation Bandwidth [1:0]

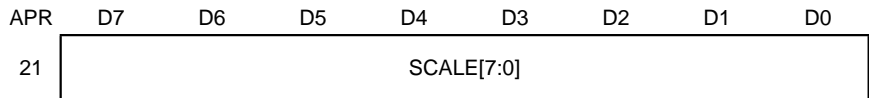
Program these bits to set the power estimation bandwidth. For more information see Section 5.7.2, “Power Control Loop.”

D1	D0	Symbol Rate (MHz)
0	0	20 - 45
0	1	10 - 20
1	0	5 - 10
1	1	2 - 5

**3.6.19
Group 4,
APR 21
Scale Factor for
DEMI and
DEMQ Outputs**

Program these bits to set the scale factor for the DEMI and DEMQ outputs from the Demodulator to the FEC Decoder. For a relationship between SCALE and PWR_REF, see Section 5.8, “Output Control.”

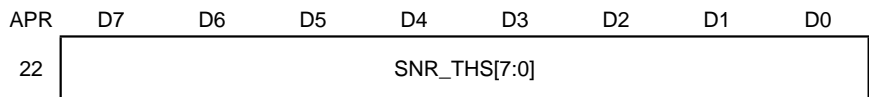
Read/Write: R/W



**3.6.20
Group 4,
APR 22
SNR Estimator
Threshold**

Use this register to set the value that the phase detector’s Signal to Noise Ratio (SNR) comparator uses as a threshold when deciding which gain value to use. For details, see Figure 5.7 in Section 5.6.2, “Carrier Phase Tracking.”

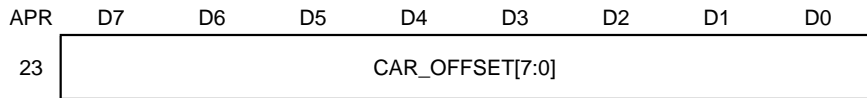
Read/Write: R/W



**3.6.21
Group 4,
APR 23
Carrier Loop DC
Offset
Compensation
Value**

Use this register to establish a DC offset voltage that is added to or subtracted from the carrier loop voltage. The value stored in this register is a signed integer that ranges from -128 to +127. For details, see Section 5.9.1, “Carrier Loop DC Offset Compensation.”

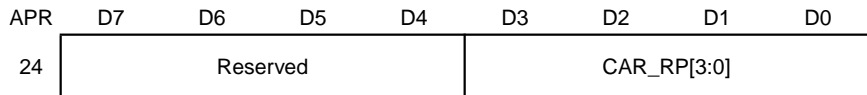
Read/Write: R/W



3.6.22
Group 4,
APR 24
Carrier
Frequency
Reference
Period

This register is used to program the preset value for the frequency sweep reference counter.

Read/Write: R/W



Reserved **Reserved Bits** **[7:4]**

These bits are reserved for LSI Logic internal use only. Reserved bits should always be set to 0, and will produce random results when read.

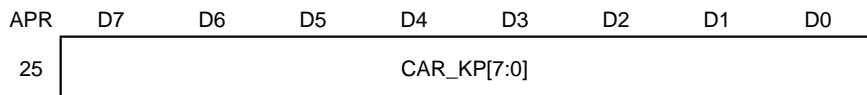
CAR_RP[3:0] Reference Period for Carrier Frequency (CAR_DCLKP/N pin) Measurement **[3:0]**

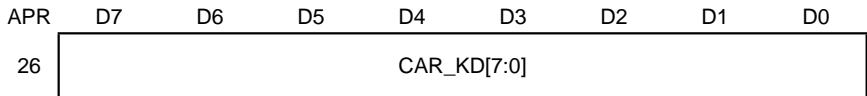
Program the preset value for the four MSBs of the frequency sweep reference counter into this register. The value programmed equals 1024 times the number of crystal (XOIN) clock cycles. See Section 5.6.1, “Carrier Acquisition.”

3.6.23
Group 4,
APR 25, 26
Carrier Loop
Filter Gain
(P and D Terms)

Program CAR_KP and CAR_KD with values that set the parameters of the carrier recovery loop. CAR_KP is restricted to values between 30 and 127 inclusive. See Section 5.6.2.2, “Loop Characteristics” for details.

Read/Write: R/W

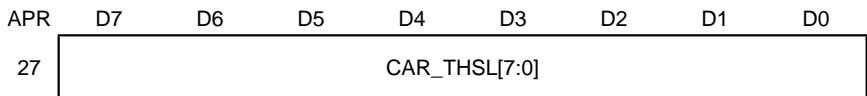




3.6.24
Group 4,
APR 27
Carrier Lock
Detector
Threshold

The value that you program into CAR_THSL determines the threshold for the Carrier Phase Lock Detector. For details, see Section 5.6.1.5, “Phase Lock Detection.”

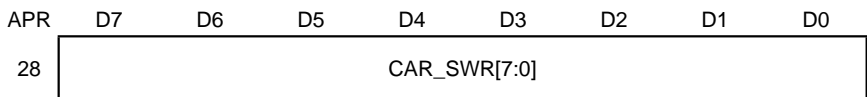
Read/Write: R/W



3.6.25
Group 4,
APR 28
Carrier
Synchronizer
Sweep Rate

The value that you program into this register determines the Carrier Synchronizer sweep rate. For details, see Section 5.6.1.4, “Frequency Sweep Rate.”

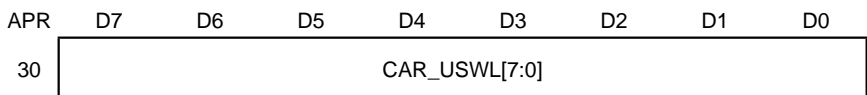
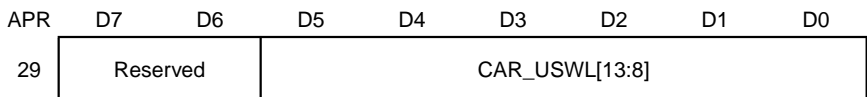
Read/Write: R/W



3.6.26
Group 4,
APR 29, 30
Carrier
Synchronizer
Sweep Upper
Limit

You program the CAR_USWL and CAR_LSWL registers to set the upper and lower limits, respectively, of the frequency sweep. For details, see Section 5.6.1.1, “Frequency Sweep Limits.”

Read/Write: R/W



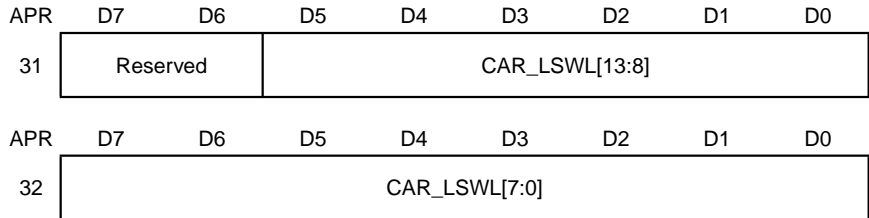
Reserved **Reserved Bits** **[7:6]**
These bits are reserved for LSI Logic internal use only.
Reserved bits should always be set to 0, and will produce
random results when read.

CAR_USWL[13:0] **Carrier Sweep Upper Sweep Limit** **[5:0], [7:0]**
Program the CAR_USWL register to set the upper limit of
the frequency sweep.

3.6.27
Group 4,
APR 31, 32
Carrier
Synchronizer
Sweep Lower
Limit

You program the CAR_USWL and CAR_LSWL registers to set the upper and lower limits, respectively, of the frequency sweep. For details, see Section 5.6.1.1, “Frequency Sweep Limits.”

Read/Write: R/W



Reserved **Reserved Bits** **[7:6]**

These bits are reserved for LSI Logic internal use only. Reserved bits should always be set to 0, and will produce random results when read.

CAR_LSWL[13:0]

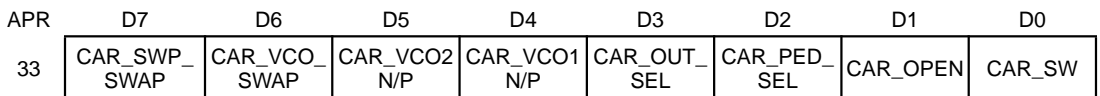
Carrier Sweep Lower Sweep Limit **[5:0], [7:0]**

Program the CAR_LSWL register to set the lower limit of the frequency sweep.

3.6.28
Group 4,
APR 33
Carrier Loop
Configuration
Register

This register contains the various control bits that are used to configure the Carrier Loop Synchronizer Loop logic. For more information, see Section 5.6, “Carrier Synchronizer.”

Read/Write: R/W



CAR_SWP_SWAP

Swap Carrier Sweep Direction **7**

Set this bit to control whether the carrier acquisition frequency sweep direction is normal or reversed. It should be toggled whenever the carrier sweep reaches its limit

without achieving carrier lock, or when the constellation has locked at 45°.

D7 Sweep Direction

0 Normal
1 Reversed

CAR_VCO_SWAP

Swap VCO Output Polarity **6**

Set this bit to invert the polarities of the CAR_VCOxN/P pins. It should be toggled whenever the carrier sweep reaches its limit without achieving carrier lock, or when the constellation has locked at 45°.

D6 Polarity

0 Normal
1 Swapped (N and P Inverted)

CAR_VCO2N/P

Outputs Active or 3-state **5**

Program this bit to enable or disable the outputs of the second Sigma Delta differential pair. For low bit rate applications that use an external DAC, you must enable both Sigma-Delta outputs by setting Carrier Loop Configuration Register bits [5:4] to zero. For more information, see Section 5.6, “Carrier Synchronizer.”

D5 CAR_VCO2N/P Pins

0 Active
1 3-state

This bit should always be set to 0 when CAR_OUT_SEL is set to 1.

CAR_VCO1N/P

Outputs Active or 3-state **4**

Program this bit to enable or disable the outputs of the first Sigma Delta differential pair. For low bit rate applications that use an external DAC, you must enable both Sigma-Delta outputs by setting Carrier Loop Configuration

Register bits [5:4] to zero. For more information, see Section 5.6, “Carrier Synchronizer.”

D4 CAR_VCO1N/P Pins

0	Active
1	3-state

This bit should always be set to 0 when CAR_OUT_SEL is set to 1.

CAR_OUT_SEL

Carrier Loop Output Selector 3

Use this bit to route the Phase Error Detector outputs to the Carrier Loop output pins instead of the Sigma-Delta circuit outputs. This allows a full range of frequencies to be decoded by using an external DAC for low baud rate operation. For more information, see Section 5.6.2.3, “Low Baud Rate Operation.”

The output pin assignments when using the CAR_OUT_SEL bit are:

Output Pin Name	CAR_OUT_SEL	
	0	1
CAR_PED.0	CAR_PED.0	CAR_PED.0
CAR_PED.1	CAR_PED.1	CAR_PED.1
CAR_VCO1P	CAR_VCO1P	CAR_PED.2
CAR_VCO2P	CAR_VCO2P	CAR_PED.3
CAR_VCO1N	CAR_VCO1N	CAR_PED.4
CAR_VCO2N	CAR_VCO2N	CAR_PED.5

CAR_PED_SEL

Carrier Phase Error Detector Select 2

Program this bit to select which phase error estimator will be used for carrier phase tracking. For details, see Section 5.6.2, “Carrier Phase Tracking,” and Figure 5.9.

D2 Estimator Selected

0	Decision Directed Maximum Likelihood (DDML)
1	Non-Data Aided Maximum Likelihood (NDAML)

CAR_OPEN **Carrier Loop Open** **1**
 Set this bit to force the loop out of a false lock condition.
 For more information see Section 5.6.1.7, “False Locks.”

D1 **Definition**

0	Enable the Carrier Loop
1	Unlock (Disable) the Carrier Loop

CAR_SW **Sweep On/off for Carrier Loop** **0**
 Set the CAR_SW bit to enable the carrier acquisition sweep generator. For more information see Section 5.6.1, “Carrier Acquisition.”

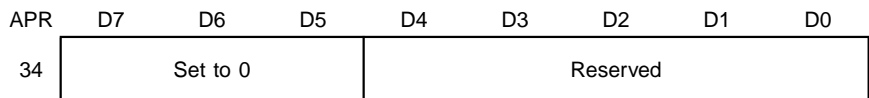
D0 **Definition**

0	Sweep Off
1	Sweep On

3.6.29
Group 4,
APR 34
Set to 0

This register is reserved for LSI Logic internal use only. You must program the bits as shown during device initialization.

Read/Write: R/W



Set to 0 **Set to 0** **[7:5]**
 You must set these bits to 0 for normal operation.

Reserved **Reserved Bits** **[4:0]**
 These bits are reserved for LSI Logic internal use only. Reserved bits should always be set to 0, and will produce random results when read.

3.6.30
Group 4,
APR 35
Decoder
Configuration
Register

This register contains the various control bits that are used to configure the L64704 Decoder logic.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
35	SNR_EST	CON_SEL	Set to 0	FP_LOCK_LEN	PWRP	Set to 0		I_FORMAT

SNR_EST **SNR Estimator On/Off** **7**
Set this bit to enable or disable the SNR Estimator circuit.

D7 SNR Estimator

0 Off
1 On

CON_SEL **Constellation Selector** **6**
Set this bit to indicate the format of the input data.

D6 Definition

0 QPSK
1 BPSK

Set to 0 **Set to 0** **5**
You must set this bit to 0 for normal operation

FP_LOCK_LEN **Frequency/Phase Lock Detector Length** **4**
Program this bit in conjunction with the Carrier Threshold field (Group 4, APR 27) to set the phase lock detector estimation period. For details, see Section [5.6.1.5](#), “Phase Lock Detection.”

D4 Estimation Period

0 Normal (Long)
1 Short

PWRP **PWRP Signal Invert** **3**
 Set this bit to invert the polarity of the signal that is output on the PWRP pin.

D4 PWRP Output Pin

0 Normal
 1 Inverted

Set to 0 **Set to 0** **[2:1]**
 You must set these bits to 0 for normal operation

I_FORMAT **Input Format Selector** **0**
 Program this bit to tell the L64704 the format of the incoming data.

D0 Input Format

0 RI and RQ in Offset Binary Format
 1 RI and RQ in 2's Complement Format

3.6.31
Group 4,
APR 36
External Output
Control Bits and
Reset Register

This register contains the control bits for the external output pins XCTR_OUT[3:0] and the bits that reset the demodulator and FEC circuitry.

Read/Write: R/W

APR	D7	D6	D5	D4	D3	D2	D1	D0
36	Reserved		XCTR[3:0]			DEMOD_ RST	FEC_ RST	

Reserved **Reserved Bits** **[7:6]**
 These bits are reserved for LSI Logic internal use only. Reserved bits should always be set to 0, and will produce random results when read.

XCTR[3:0] **External Control Output Bits** **[5:2]**
 The value that you set on a bit in this field will appear on the corresponding external output pin XCTR_OUT[3:0]. See [Section 5.9.2, "External Controls,"](#) for more information.

XCTR	Definition
0	Corresponding Output Pin = VSS
1	Corresponding Output Pin = VDD

DEMOD_RST QPSK Demodulator Software Reset 1

The L64704 resets the internal datapath and control modules for the QPSK Demodulator portion of the device when you set the DEMOD_RST bit to 1. The FEC decoder module is not affected. You do not need to set the bit back to 0 to complete the reset. The L64704 issues a single reset pulse each time the microcontroller writes a one to this bit. When the DEMOD_RST bit is set, the L64704 resets the demodulator processing unit and state machines to their initial states.

Demod_Reset	Definition
0	No Reset
1	L64704 Issues a Demodulator Reset

FEC_RST FEC Decoder Software Reset 0

The L64704 resets the internal datapath and control modules for the FEC portion of the device when you set the FEC_RST bit to 1. The demodulator module is not affected. You do not need to set the bit back to 0 to complete the reset. The L64704 issues a single reset pulse each time the microcontroller writes a one to this bit. When the FEC_RST bit is set, the L64704 resets the FEC processing unit and state machines to their initial states.

FEC_Reset	Definition
0	No Reset
1	L64704 Issues an FEC Reset

Chapter 4

Channel Interfaces and Data Control

The L64704 interface supports two independent interfaces for incoming channel data and for decoded output data. Both interfaces are used simultaneously. The input interface transfers data from an external ADC device to the L64704. The output interface transfers data from the L64704 to the next processing device, typically an MPEG-2 transport demultiplexer such as LSI Logic's L64007. This chapter contains five sections:

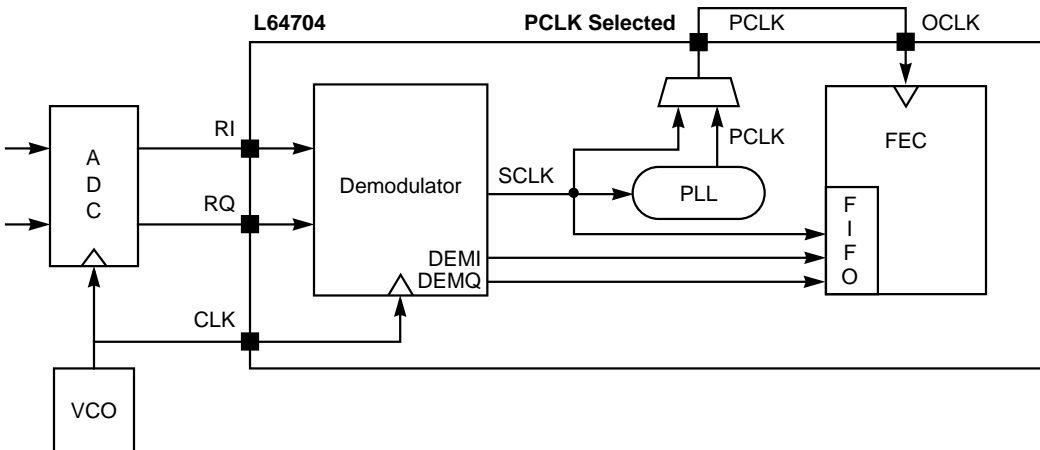
- ◆ [Section 4.1, "Data Control and Clocking Schemes,"](#) describes the Channel Data Interface signals and the clock that strobes data into the L64704.
- ◆ [Section 4.2, "Channel Data Input Interface,"](#) provides timing diagrams for the Channel Data input signals.
- ◆ [Section 4.3, "Channel Data Output Interface,"](#) provides timing diagrams for the Channel Data output signals.
- ◆ [Section 4.4, "PLL Clock Generation,"](#) describes the Phase-Locked Loop clock generation circuitry in detail.
- ◆ [Section 4.5, "Data Path Output Configurations,"](#) shows how to program the output data path multiplexer to carry the outputs of the various stages of the decoding pipeline.

4.1 Data Control and Clocking Schemes

The L64704 uses two input clock signals, CLK and OCLK, to accommodate a number of possible configurations in a channel decoding system. CLK is generated by the external Clock VCO and can be two, three, or four times the symbol rate. There is also an internally generated symbol clock, SCLK.

OCLK is the Forward Error Correction clock. Its relation to CLK is determined by the Viterbi puncture rate and the number of samples per symbol at the ADC. An on-chip PLL generates the desired OCLK frequency and outputs it to the PCLK output pin (see [Figure 4.1](#)). You should connect the PCLK output pin to the OCLK input pin.

Figure 4.1
L64704 Clocking:
Internal PLL



You can also generate the desired OCLK signal using an external PLL (see [Figure 4.2](#)). In that case the PCLK pin should be set to output the symbol rate clock, SCLK. The external PLL frequency is a function of the Viterbi puncture rate.

Figure 4.2
L64704 Clocking:
External PLL

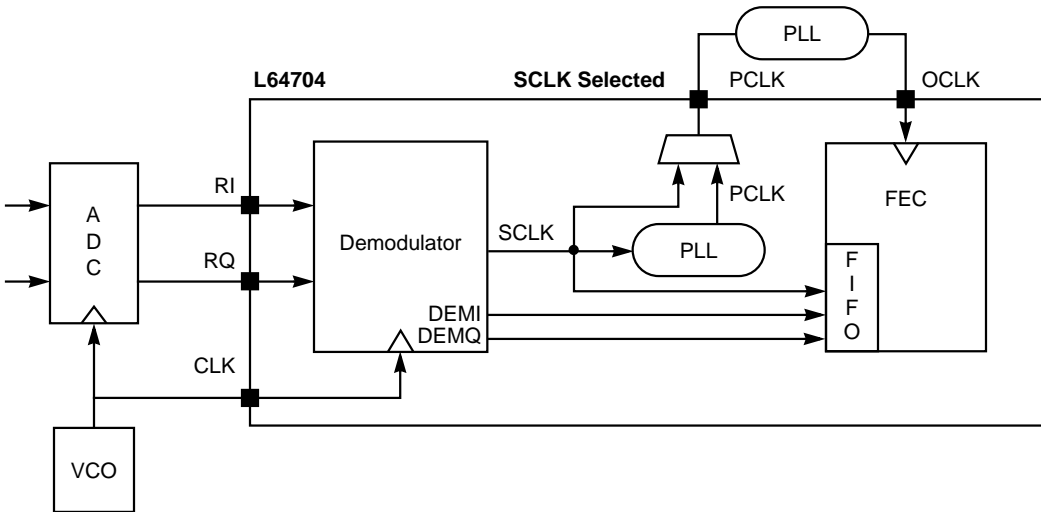


Figure 4.3 and Figure 4.4 show several clocking examples. Figure 4.3 shows a case where the input data rate is 1/2 the data processing rate in the decoding pipeline. The FEC FIFO input and FIFO output data streams run at the same rate because no extra information (erasures) need to be added after the FIFO. The CLK and OCLK signals do not need to be aligned in phase.

Figure 4.3
Code Rate = 1/2
System

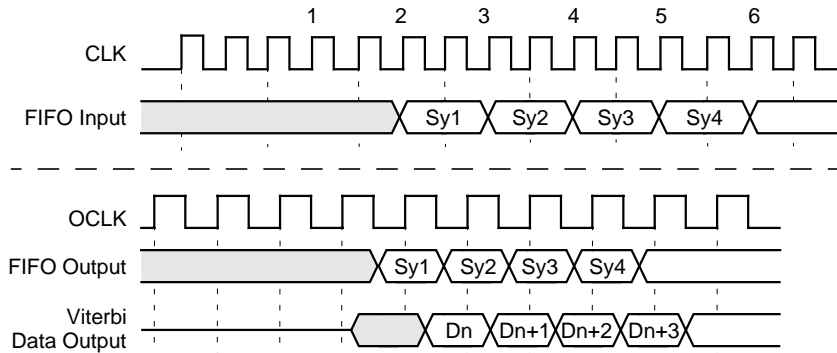


Figure 4.4 illustrates a case where the input data rate is set to 3/4 of the data processing rate in the decoding pipeline. Because the depuncturing logic inserts extra symbols (erasures), the L64704 transmits the symbols from the FIFO in small bursts at the higher clock rate (OCLK). After leaving the Viterbi Decoder, the data stream becomes continuous at the OCLK rate.

Figure 4.4
Code Rate = 3/4
System; Different
OCLK and CLK

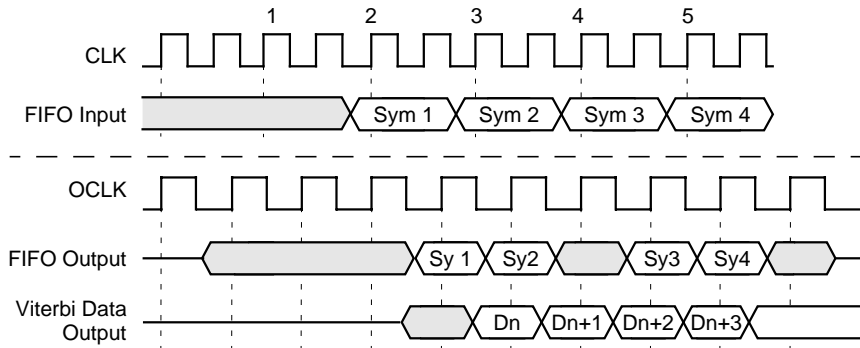
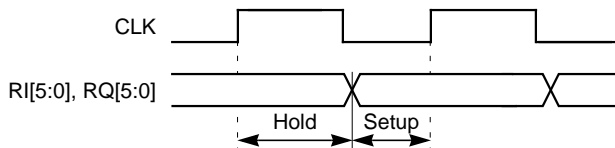


Figure 4.4 shows a case in which the data rate ratios shown are maintained, the incoming data stream is continuous, and the decoder fixes the frequency of OCLK at twice that of CLK. Because the decoder reads the FIFO at the OCLK frequency—which is greater than the Viterbi code rate—the FIFO empties periodically. The data pipeline is designed to handle such internal interruptions in the data stream without corrupting data that is already being processed. As a consequence, the channel output data appears in bursts at the OCLK rate, but on average maintains the data rate imposed by the Viterbi Decoder. The DVALIDOUT signal indicates when valid data is on the CO[7:0] output.

4.2 Channel Data Input Interface

Figure 4.5 shows how the channel data input signals RI[5:0] and RQ[5:0] are referenced to CLK.

Figure 4.5
CLK Reference to
Channel Data Input



4.3 Channel Data Output Interface

Figure 4.6
OCLK Reference to Channel Data Output

Figure 4.6 shows how the channel data output signals CO[7:0], DVALIDOUT, $\overline{\text{ERROROUT}}$, and FSTARTOUT are referenced to OCLK.

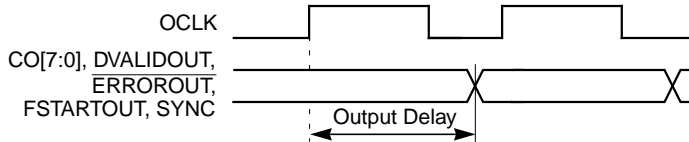
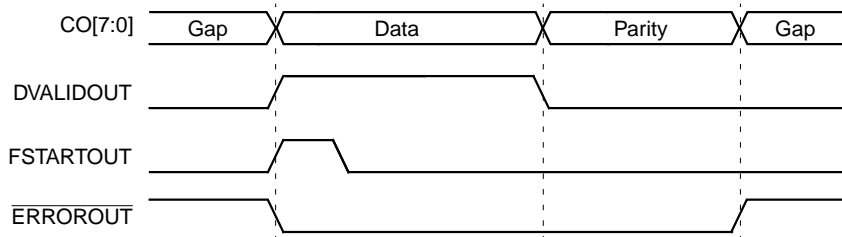


Figure 4.7 shows that new data is valid on the output whenever the L64704 asserts DVALIDOUT. The L64704 deasserts DVALIDOUT when it transfers parity and gap data. When the L64704 detects an uncorrectable error, it asserts $\overline{\text{ERROROUT}}$ while it transmits both data and parity bytes.

Figure 4.7
FSTARTOUT Related to Symbols



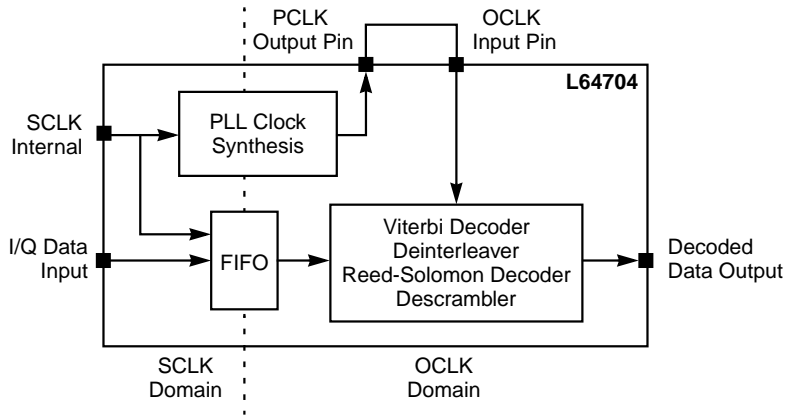
The L64704 asserts FSTARTOUT when it transfers the first bit of the first symbol of every frame. The frame structure does not require a gap, and the decoding process does not affect the gap bytes.

4.4 PLL Clock Generation

The data control and clocking schemes presented in [Section 4.1, "Data Control and Clocking Schemes,"](#) outline the requirements for the generation of the two external clock signals (CLK and OCLK) that are required by the L64704. You have to choose whether to provide an externally generated clock to the OCLK input or to use the internal PLL for clock synthesis. The internal PLL is selected by connecting the PLL output pin (PCLK) to the OCLK input pin as shown in [Figure 4.8](#) and in [Figure 4.1](#).

Using the internal PLL clock feature allows the L64704 to consume the minimum amount of power.

Figure 4.8
PLL Clock
Generation



The L64704 contains a clock synthesizer to derive OCLK from SCLK operating in the range of 2 MHz to 62.5 MHz (see [Figure 4.9](#)). The synthesized clock is available on the PCLK output pin.

The PLL can be configured to handle clock ratios for the Viterbi code rates of 1/2, 2/3, 3/4, 5/6, and 7/8. The following four registers must be set to derive the appropriate clock frequencies:

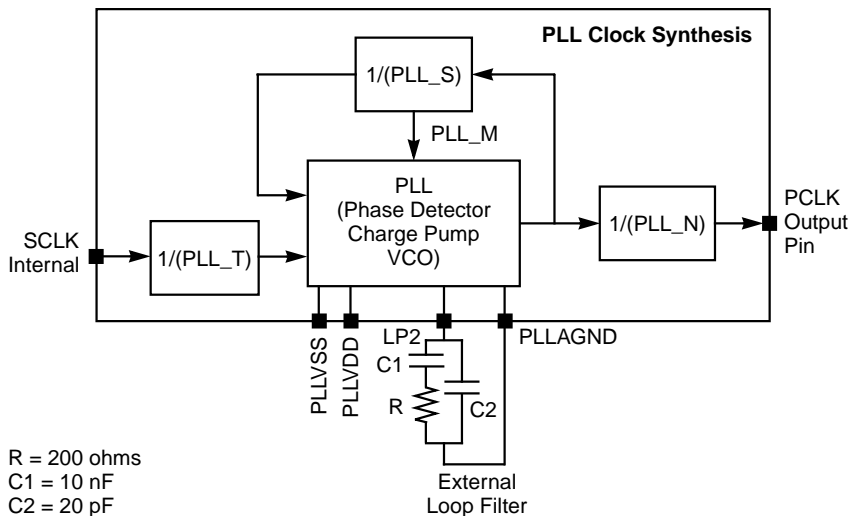
- ◆ PLL_T[4:0], Group 4, APR 2
- ◆ PLL_N[5:0], Group 4, APR 0
- ◆ PLL_S[5:0], Group 4, APR 1
- ◆ PLL_M[1:0], Group 4, APR 3

Table 4.1 shows the ratio of CLK to SCLK.

Table 4.1
CLK/SCLK Ratio

CLK_RATIO[2:0] Group 4, APR 18	CLK_DR[1:0] Group 4, APR 14	Ratio CLK/SCLK
0	0	2
1	0	4
2	0	8
3	0	16
4	0	32
0	1	4
1	1	8
2	1	16
3	1	32
4	1	64
0	2	3
1	2	6
2	2	12
3	2	24
4	2	48

Figure 4.9
PLL Clock
Synthesis



The recommended values for PLL_S, PLL_N, PLL_T, and PLL_M to cover the frequency range from 2 to 62.5 MHz for PCLK are tabulated in Table 4.2.

Table 4.2
 Values for PLL_S,
 PLL_N, PLL_T, and
 PLL_M

Code Rate	PLL_S[5:0]	PLL_N[5:0]	PLL_T[4:0]	PLL_M[1:0]	VCO		SCLK		PCLK	
					Min	Max	Min	Max	Min	Max
1/2	2	1	2	3	70	80	70.00	80.00	70.00 ¹	80.00 ¹
				2	60	70	60.00	70.00	60.00	70.00 ¹
				1	50	60	50.00	60.00	50.00	60.00
				0	40	50	40.00	50.00	40.00	50.00
	4	2	2	3	70	80	35.00	40.00	35.00	40.00
				2	60	70	30.00	35.00	30.00	35.00
				1	50	60	25.00	30.00	25.00	30.00
				0	40	50	20.00	25.00	20.00	25.00
	8	4	2	3	70	80	17.50	20.00	17.50	20.00
				2	60	70	15.00	17.50	15.00	17.50
				1	50	60	12.50	15.00	12.50	15.00
	12	6	2	3	70	80	11.67	13.33	11.67	13.33
				2	60	70	10.00	11.67	10.00	11.67
	16	8	2	3	70	80	8.75	10.00	8.75	10.00
				2	60	70	7.50	8.75	7.50	8.75
				1	50	60	6.25	7.50	6.25	7.50
				0	40	50	5.00	6.25	5.00	6.25
	20	10	2	0	40	50	4.00	5.00	4.00	5.00
	24	12	2	0	40	50	3.33	4.17	3.33	4.17
	28	14	2	0	40	50	2.86	3.57	2.86	3.57
32	16	2	0	40	50	2.50	3.12	2.50	3.12	
36	18	2	0	40	50	2.22	2.78	2.22	2.78	
40	20	2	0	40	50	2.00	2.50	2.00	2.50	

(Sheet 1 of 4)

Table 4.2 (Cont.)
 Values for PLL_S,
 PLL_N, PLL_T, and
 PLL_M

Code Rate	PLL_S[5:0]	PLL_N[5:0]	PLL_T[4:0]	PLL_M[1:0]	VCO		SCLK		PCLK				
					Min	Max	Min	Max	Min	Max			
2/3	8	1	6	3	70	80	52.50	60.00	70.00 ¹	80.00 ¹			
				2	60	70	45.00	52.50	60.00	70.00 ¹			
				1	50	60	37.50	45.00	50.00	60.00			
				0	40	50	30.00	37.50	40.00	50.00			
	16	2	6	3	70	80	26.25	30.00	35.00	40.00			
				2	60	70	22.50	26.25	30.00	35.00			
				1	50	60	18.75	22.50	25.00	30.00			
				0	40	50	15.00	18.75	20.00	25.00			
		6	2	1	50	60	6.25	7.50	8.33	10.00			
				0	40	50	5.00	6.25	6.67	8.33			
				32	4	6	3	70	80	13.12	15.00	17.50	20.00
							2	60	70	11.25	13.12	15.00	17.50
	1	50	60				9.38	11.25	12.50	15.00			
	0	40	50				7.50	9.38	10.00	12.50			
	12	2	3	70	80	4.38	5.00	5.83	6.67				
			2	60	70	3.75	4.38	5.00	5.83				
			1	50	60	3.12	3.75	4.17	5.00				
			0	40	50	2.50	3.12	3.33	4.17				
	48	18	2	1	50	60	2.08	2.50	2.78	3.33			
				0	48	50	2.00	2.08	2.67	2.78			
3/4	6	1	4	3	70	80	46.67	53.33	70.00 ¹	80.00 ¹			
				2	60	70	40.00	46.67	60.00	70.00 ¹			
				1	50	60	33.33	40.00	50.00	60.00			
				0	40	50	26.67	33.33	40.00	50.00			
	2	2	3	70	80	23.33	26.67	35.00	40.00				
			2	60	70	20.00	23.33	30.00	35.00				
			1	50	60	16.67	20.00	25.00	30.00				
			0	40	50	13.33	16.67	20.00	25.00				

(Sheet 2 of 4)

Table 4.2 (Cont.)
 Values for PLL_S,
 PLL_N, PLL_T, and
 PLL_M

Code Rate	PLL_S[5:0]	PLL_N[5:0]	PLL_T[4:0]	PLL_M[1:0]	VCO		SCLK		PCLK	
					Min	Max	Min	Max	Min	Max
3/4	12	4	2	3	70	80	11.67	13.33	17.50	20.00
				2	60	70	10.00	11.67	15.00	17.50
				1	50	60	8.33	10.00	12.50	15.00
				0	40	50	6.67	8.33	10.00	12.50
	18	6	2	1	50	60	5.56	6.67	8.33	10.00
	24	8	2	2	60	70	5.00	5.83	7.50	8.75
				1	50	60	4.17	5.00	6.25	7.50
				0	40	50	3.33	4.17	5.00	6.25
	42	14	2	2	60	70	2.86	3.33	4.29	5.00
				1	50	60	2.38	2.86	3.57	4.29
				0	42	50	2.00	2.38	3.00	3.57
	5/6	10	1	6	3	70	80	42.00	48.00	70.00 ¹
2					60	70	36.00	42.00	60.00	70.00 ¹
1					50	60	30.00	36.00	50.00	60.00
0					40	50	24.00	30.00	40.00	50.00
20		2	6	3	70	80	21.00	24.00	35.00	40.00
				2	60	70	18.00	21.00	30.00	35.00
				1	50	60	15.00	18.00	25.00	30.00
				0	40	50	12.00	15.00	20.00	25.00
		6	2	1	50	60	5.00	6.00	8.33	10.00
				0	40	50	4.00	5.00	6.67	8.33
40		4	6	3	70	80	10.50	12.00	17.50	20.00
				2	60	70	9.00	10.50	15.00	17.50
				1	50	60	7.50	9.00	12.50	15.00
				0	40	50	6.00	7.50	10.00	12.50
		12	2	3	70	80	3.50	4.00	5.83	6.67
				2	60	70	3.00	3.50	5.00	5.83
				1	50	60	2.50	3.00	4.17	5.00
				0	40	50	2.00	2.50	3.33	4.17

(Sheet 3 of 4)

Table 4.2 (Cont.)
 Values for PLL_S,
 PLL_N, PLL_T, and
 PLL_M

Code Rate	PLL_S[5:0]	PLL_N[5:0]	PLL_T[4:0]	PLL_M[1:0]	VCO		SCLK		PCLK		
					Min	Max	Min	Max	Min	Max	
7/8	14	1	8	3	70	80	40.00	45.71	70.00 ¹	80.00 ¹	
				1	50	60	28.57	34.29	50.00	60.00	
				0	40	50	22.86	28.57	40.00	50.00	
		2	4	3	70	80	20.00	22.86	35.00	40.00	
				2	60	70	17.14	20.00	30.00	35.00	
				1	50	60	14.29	17.14	25.00	30.00	
				0	40	50	11.43	14.29	20.00	25.00	
		4	2	3	70	80	10.00	11.43	17.50	20.00	
				2	60	70	8.57	10.00	15.00	17.50	
				1	50	60	7.14	8.57	12.50	15.00	
		28	8	2	3	70	80	5.00	5.71	8.75	10.00
					2	60	70	4.29	5.00	7.50	8.75
	1				50	60	3.57	4.29	6.25	7.50	
	42	6	4	3	70	80	6.67	7.62	11.67	13.33	
				2	60	70	5.71	6.67	10.00	11.67	
		12	2	3	70	80	3.33	3.81	5.83	6.67	
				2	60	70	2.86	3.33	5.00	5.83	
				1	50	60	2.38	2.86	4.17	5.00	
				0	42	50	2.00	2.38	3.50	4.17	

(Sheet 4 of 4)

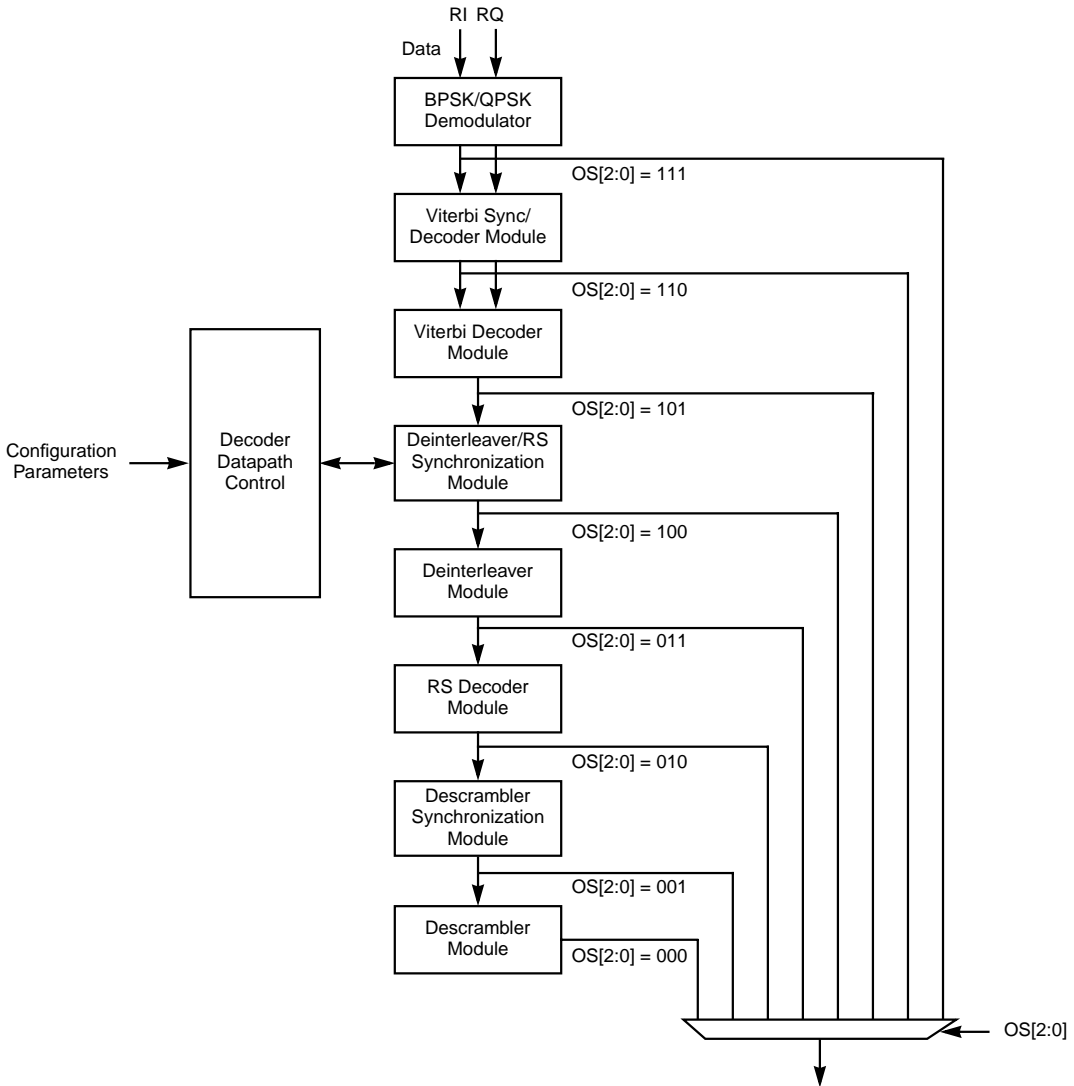
1. Although the PLL module can generate PCLK frequencies of up to 80 MHz, the maximum OCLK frequency is limited to 62.5 MHz.

4.5
Data Path
Output
Configurations

The L64704 provides the user with a mechanism to observe the output of each functional block in the decoding pipeline. This feature simplifies performance characterization and system diagnostics tasks. [Figure 4.10](#) shows the functional blocks in the decoding pipeline.

You can observe the outputs from the Descrambler, Reed-Solomon Decoder, Viterbi Decoder, Deinterleaver Module and the QPSK Demodulator through the CO[7:0], DVALIDOUT, ERROROUT, FSTARTOUT and BCLKOUT output signals. To select an output, the external microcontroller must set the output selector bits in the OS[2:0] (Group 4, APR 12) register to enable the appropriate functional block output. See the description for OS[2:0] on [page 3-36](#) for details.

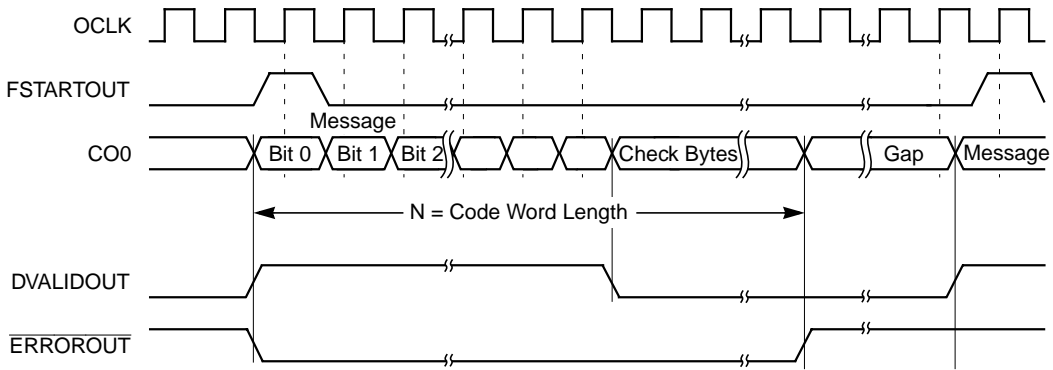
Figure 4.10
L64704 Functional
Blocks in the Decoding
Pipeline



4.5.1 Descrambler Output

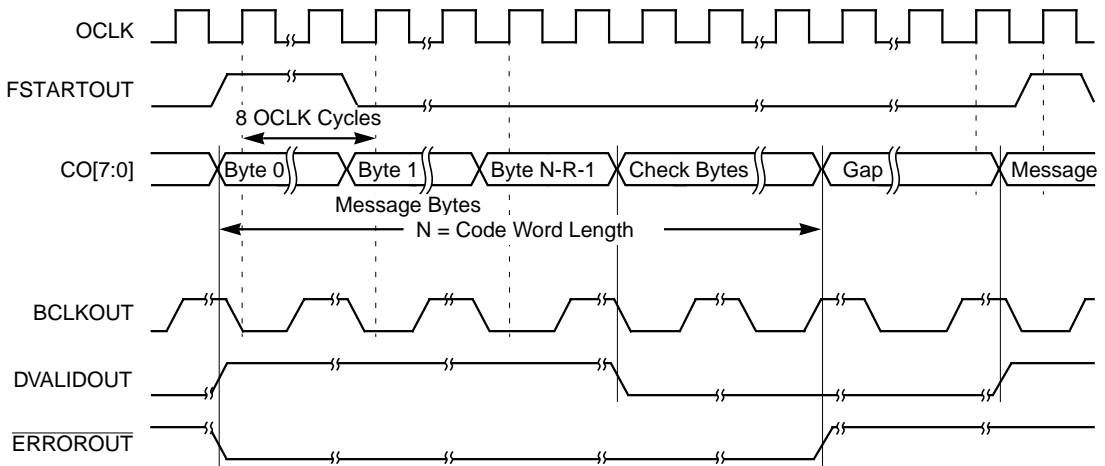
You can observe the output of the entire decoding pipeline, ending after the Descrambler, by setting the OS[2:0] bits to 0b000. [Figure 4.11](#) and [Figure 4.12](#) show the Descrambler output waveforms for Serial Channel Output Mode and Parallel Channel Output Mode respectively.

Figure 4.11
Descrambler Serial
Output Waveforms



When you set the Output Format bit (Group 4, APR 12) to 0 (Serial Channel Output Mode), the L64704 outputs data bit serially on CO[0]. The L64704 outputs new data one bit per cycle of OCLK (see [Figure 4.11](#)). The L64704 asserts FSTARTOUT for one cycle that overlaps the first message bit of a Reed-Solomon code word.

Figure 4.12
Descrambler Parallel
Output Format



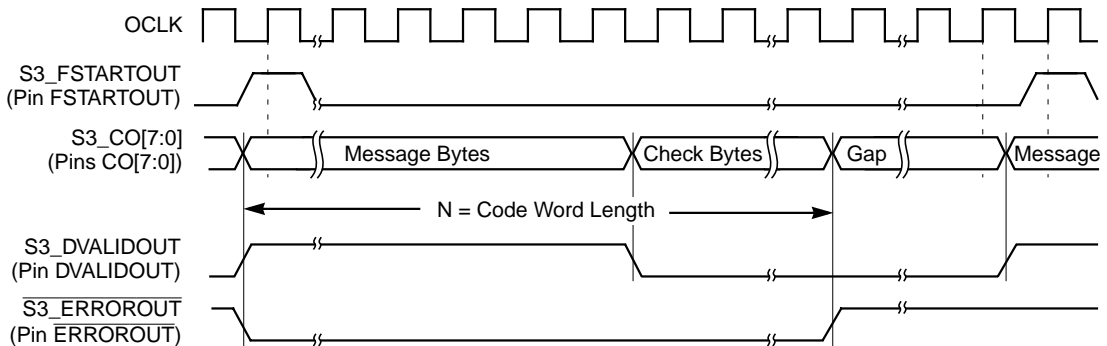
When you set the OF bit to 1 (Parallel Channel Output Mode), the L64704 outputs one new data byte on CO[7:0] every eight OCLK cycles ([Figure 4.12](#)). The L64704 chronologically orders the data in Parallel

Channel Output Mode, where the MSB is oldest, and the LSB is newest. The FSTARTOUT strobe overlaps the first data byte. If BF is set (Group 4, APR 11), the L64704 provides BCLKOUT as an additional strobe that has one rising and one falling edge per valid CO[7:0] data byte. The L64704 asserts BCLKOUT in the middle of the decoded data bytes, so the device that receives the output from the L64704 can latch data at the BCLKOUT rate rather than at the OCLK rate. BCLKOUT is a continuous clock output at 1/8 the OCLK frequency when BF is cleared, regardless of whether data is present on the CO[7:0] bus.

4.5.2 Synchronization Stage 3 Output

You can observe the outputs of the synchronization stage preceding the Descrambler by setting the OS[2:0] bits to 0b001. [Figure 4.13](#) shows the Synchronization Stage 3 output signals. Signals prefixed by “S3_” are driven on the pin indicated in parenthesis below the signal name.

Figure 4.13
Synchronization
Stage 3 Output
Waveforms

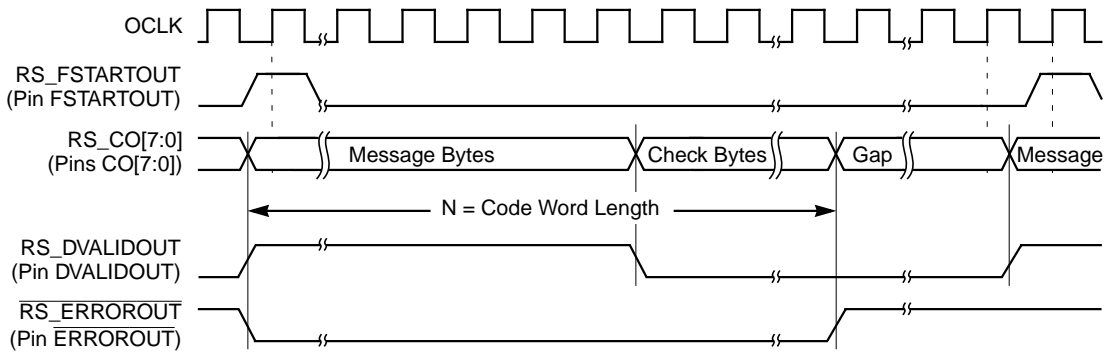


In contrast to the Descrambler output, the CO[7:0] bus still carries scrambled data.

4.5.3 Reed-Solomon Decoder Output

You can observe the outputs of the Reed-Solomon decoder module by setting the OS[2:0] bits to 0b010. This mode can also be used if you want to bypass the Descrambler entirely. [Figure 4.14](#) shows the Reed-Solomon Decoder output signals. Signals prefixed by “RS_” are driven on the pin indicated in parenthesis below the signal name.

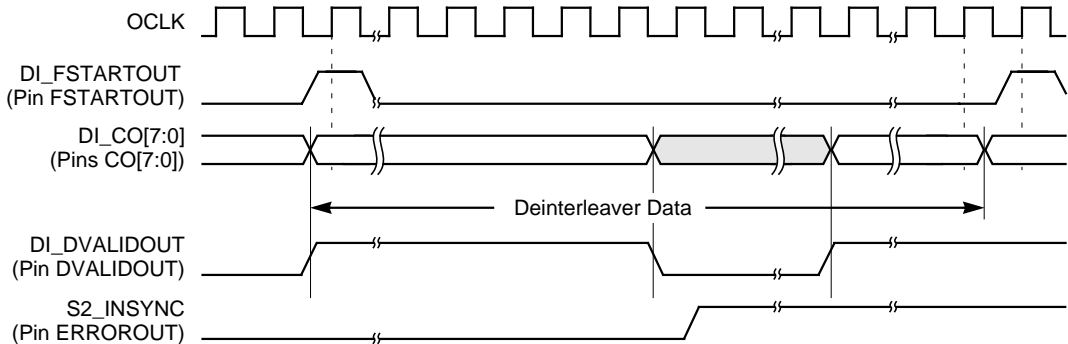
Figure 4.14
Reed-Solomon
Decoder Output
Waveforms



4.5.4
Deinterleaver
Output

You can observe the output signals from the Convolutional Deinterleaver by setting the OS[2:0] bits to 0b011. [Figure 4.15](#) shows the Deinterleaver output waveforms. Signals prefixed by “DI_” are driven on the pin indicated in parenthesis below the signal name.

Figure 4.15
Deinterleaver Output
Waveforms

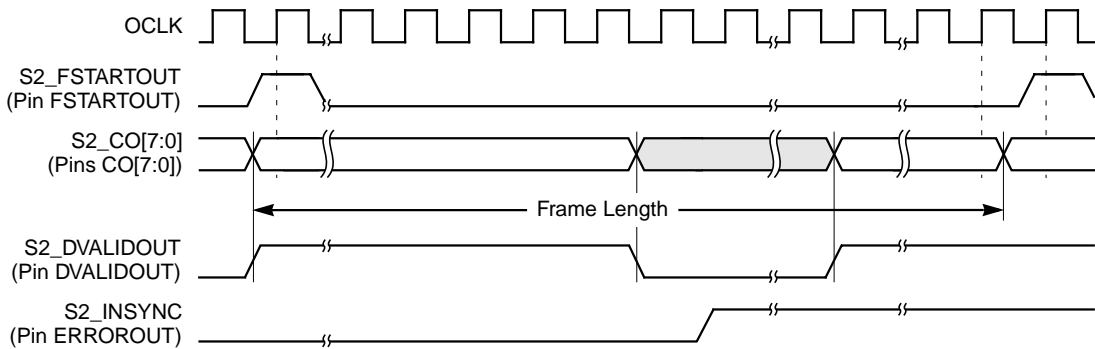


The L64704 uses the FSTARTOUT, CO[7:0], and DVALIDOUT signals to carry the corresponding Deinterleaver outputs.

4.5.5 Synchronization Stage 2 Output

You can observe the output of the synchronization stage preceding the Deinterleaver by setting the OS[2:0] bits to 0b100. Synchronization Stage 2 detects the predefined synchronization word to properly align the data stream. Figure 4.16 shows the waveforms for the Synchronization Stage 2 output signals. Signals prefixed by “S2_” are driven on the pin indicated in parenthesis below the signal name.

Figure 4.16
Synchronization
Stage 2 Output
Waveforms

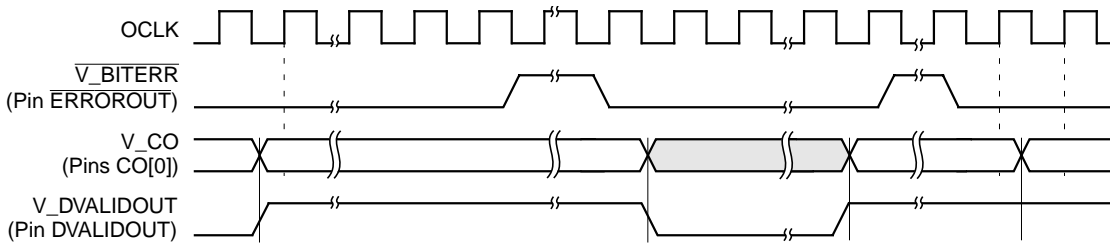


You can observe the S2_INSYNC signal to monitor the state of the second synchronization stage. When the L64704 asserts S2_INSYNC, it indicates that the decoder has established frame synchronization. When the L64704 deasserts S2_INSYNC, it indicates an out-of-sync condition.

4.5.6 Viterbi Decoder Output

You can observe the outputs of the Viterbi decoder module by setting the OS[2:0] bits to 0b101. You use this mode to observe the decoded data after only the inner layer of decoding. Figure 4.17 shows the waveforms for the Viterbi Decoder output signals. Signals prefixed by “V_” are driven on the pin indicated in parenthesis below the signal name.

Figure 4.17
Viterbi Decoder Output
Waveforms

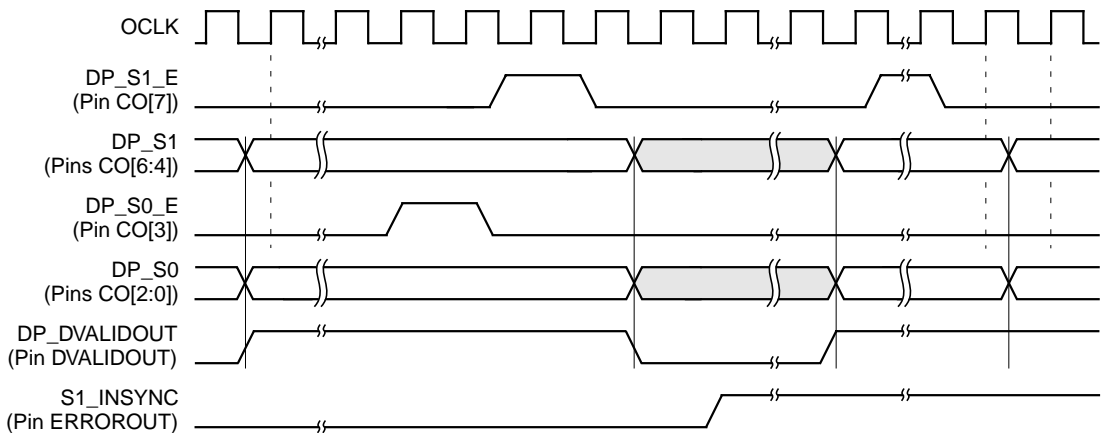


The L64704 outputs the decoded Viterbi data stream serially on pin CO0 one bit per OCLK cycle. The V_DVALIDOUT signal indicates whether data on CO0 is valid on a cycle-by-cycle basis. The $\overline{V_BITERR}$ signal carries information on errors found in the Viterbi output bit stream. If the L64704 deasserts $\overline{V_BITERR}$, it indicates that the decoder has not correctly decoded the current data on V_CO.

4.5.7
Viterbi
Depuncture/
Synchronization
Output

You can observe the outputs of the Viterbi synchronization stage and the associated depuncturing module by setting the OS[2:0] bits to 0b110. [Figure 4.18](#) shows the waveforms for the Viterbi Synchronization/Depuncture module output signals. Signals prefixed by “DP_” are driven on the pin indicated in parenthesis below the signal name.

Figure 4.18
Viterbi Depuncture/
Synchronization Output
Waveforms

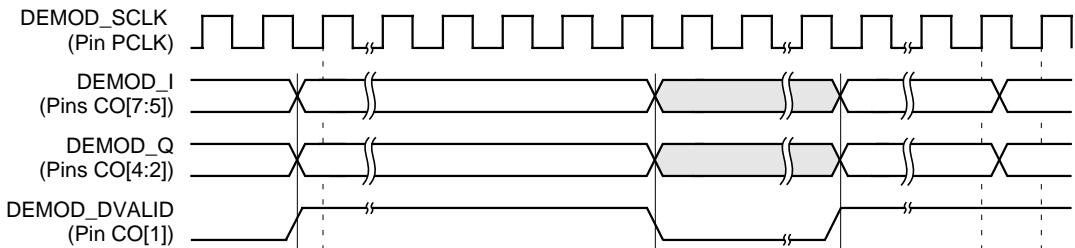


In this mode, the L64704 outputs the depunctured Viterbi input data stream. The data stream consists of two symbol streams and two corresponding erasures flags on the CO[7:0] bus as shown in [Figure 4.18](#). The L64704 uses the S1_INSYNC signal to monitor the state of the Viterbi synchronization stage. When the L64704 asserts S1_INSYNC, it indicates that Viterbi module synchronization has been established. When the L64704 deasserts S1_INSYNC, it indicates an out-of-sync condition.

4.5.8
QPSK
Demodulator
Output

You can observe the outputs of the QPSK Demodulator module by setting the OS[2:0] bits to 0b111. Signals prefixed by “DEMODO_” are driven on the pin indicated in parenthesis below the signal name. [Figure 4.19](#) shows the waveforms for the QPSK Demodulator module output signals.

Figure 4.19
 QPSK Demodulator
 Output Waveforms



In this mode, the L64704 outputs the demodulated QPSK data stream. This data stream consists of two symbol streams DEMOD_I and DEMOD_Q accompanied by DEMOD_DVALID.

Chapter 5

Demodulator Module

Functional Description

This chapter describes the function of the BPSK/QPSK Demodulator module within the L64704 and is divided into the following sections:

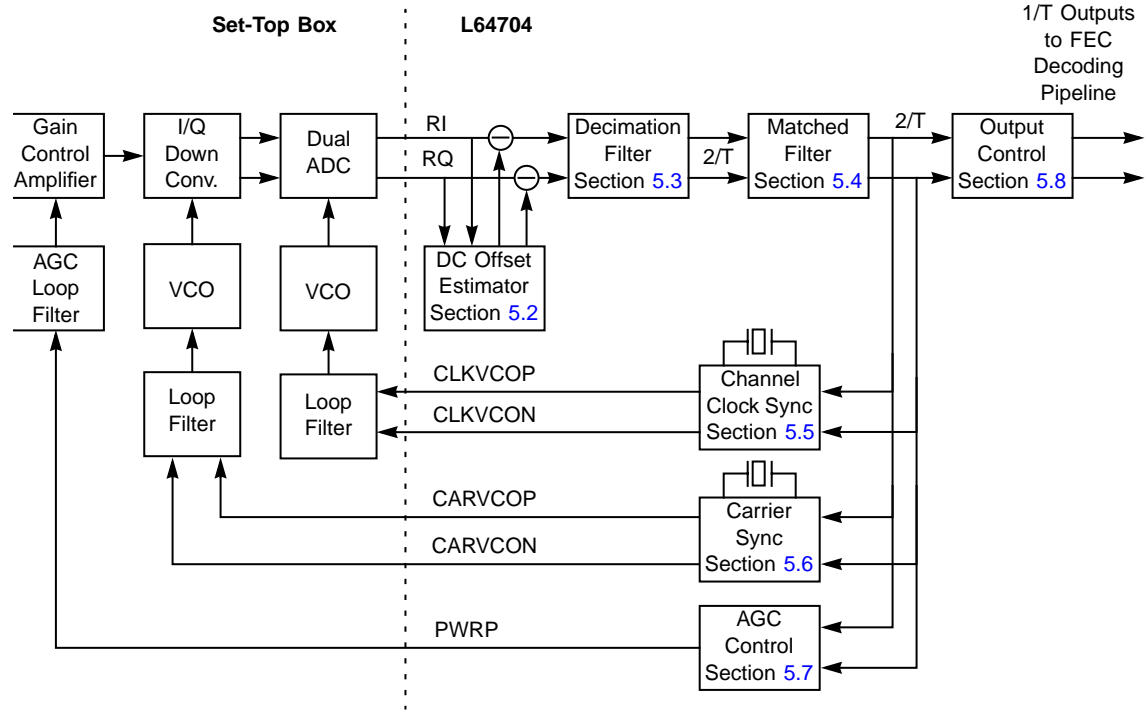
- ◆ [Section 5.1, “Overview,”](#) provides a high-level description of the Demodulator Module and shows how it fits into a set-top decoder.
- ◆ [Section 5.2, “DC Offset Compensation and Coupling to ADC Output,”](#) describes the L64704’s DC Offset Compensation circuit.
- ◆ [Section 5.3, “Decimation Filters,”](#) describes the two input decimation filters.
- ◆ [Section 5.4, “Matched Filter,”](#) provides information on the I and Q branch decimation filter.
- ◆ [Section 5.5, “Channel Clock Recovery,”](#) provides information on the Channel Clock recovery loop.
- ◆ [Section 5.6, “Carrier Synchronizer,”](#) describes the logic that is necessary to implement the Carrier Synchronizer circuit.
- ◆ [Section 5.7, “Automatic Gain Control \(AGC\),”](#) describes the L64704’s automatic gain control.
- ◆ [Section 5.8, “Output Control,”](#) provides information on the QPSK demodulator’s output control circuitry.
- ◆ [Section 5.9, “Other Functions,”](#) describes all of the remaining circuitry in the L64704’s BPSK/QPSK Demodulator.

5.1 Overview

The Demodulator Module connects to the satellite receiver circuitry in the set-top box to recover the modulated MPEG-2 transport stream.

[Figure 5.1](#) shows the connections between the BPSK/QPSK Demodulator and its associated circuitry.

Figure 5.1
Demodulator Module
and its Associated
Circuitry

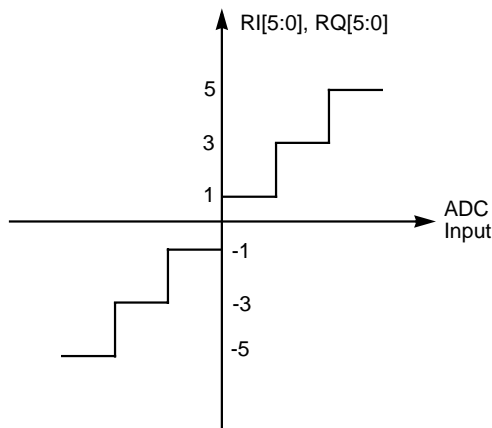


5.2 DC Offset Compensation and Coupling to ADC Output

The L64704 provides for an internal suppression of DC offsets on the I and Q channels. To enable this function, set the PWR_BW bits (Group 4, APR 20). This feature is particularly useful when using an integrated front end that does not provide DC offset compensation pins and that introduces small offsets.

The external analog to digital convertor must produce six-bit samples that reflect the 32-positive values and 32-negative values as shown in [Figure 5.2](#). The six-bit samples are fed to the RI[5:0] and RQ[5:0] inputs.

Figure 5.2
Input Quantization
with AC Coupling



5.3 Decimation Filters

The L64704 implements two switchable decimation filters on each I and Q branch: a 1/2-band filter and a 2/3-band filter. These two filters enable the Analog to Digital Converter (ADC) to operate at an oversampling ratio of $N = 2, 3, \text{ or } 4$. The filters generate $2/T$ -sampled I and Q streams from the $3/T$ or $4/T$ sampled I and Q inputs. The resulting $2/T$ streams are inputs for the matched filter.

To configure the decimation filters, the microcontroller should write one of the following values to the CLK_DR[1:0] bits of the Clock Loop Control 1 register (Group 4, APR14):

- ◆ CLK_DR = 0 for no decimation, $N = 2$
- ◆ CLK_DR = 1 for decimation by 1/2, $N = 4$
- ◆ CLK_DR = 2 for decimation by 2/3, $N = 3$

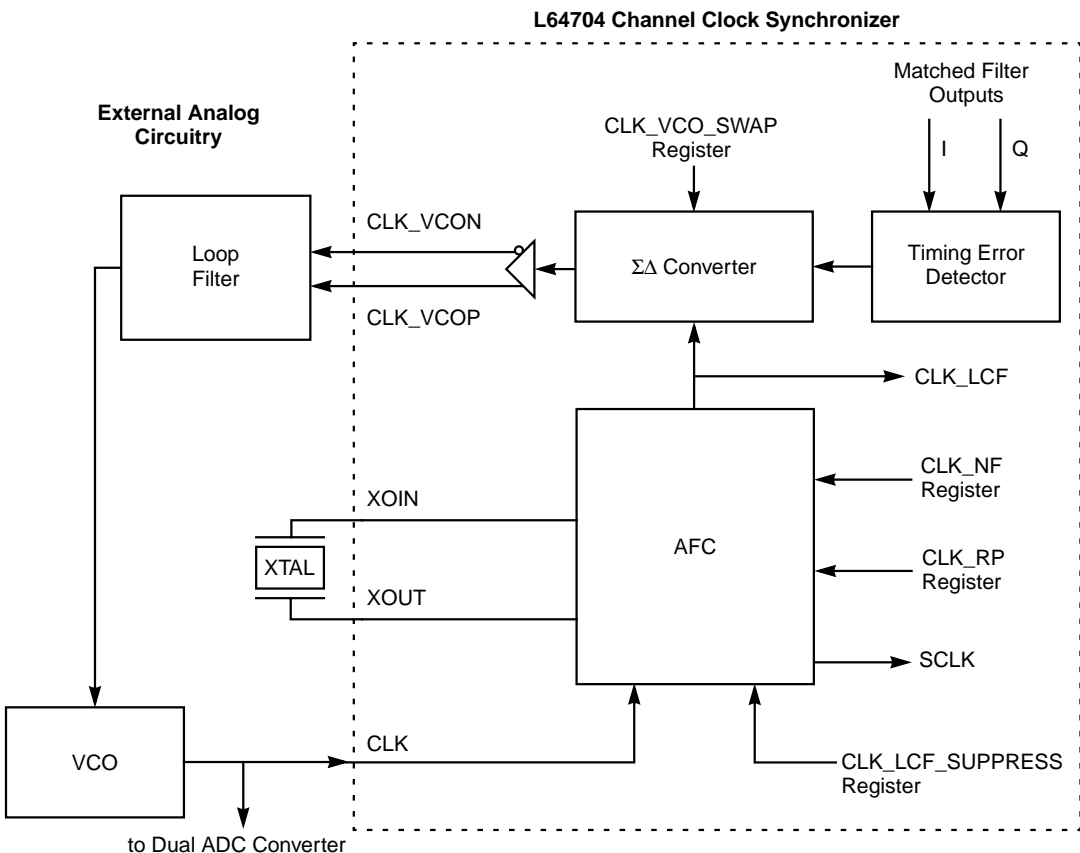
**5.4
Matched Filter**

The L64704 implements a fixed matched filter on the I and Q branches according to the DVB standard (square root raised cosine shape with roll-off $B = 0.35$). The filter operates at a constant input rate of $2/T$.

**5.5
Channel Clock
Recovery**

Figure 5.3 illustrates the Channel Clock recovery loop. This circuit consists of the L64704's Clock Synchronizer and external analog circuitry. The Clock Synchronizer generates the loop voltage for an external VCO from the L64704's matched-filtered I and Q samples. The Clock Synchronizer delivers this voltage to the two balanced CMOS differential output pins CLK_VCON and CLK_VCOP. These outputs feed the inverting and noninverting inputs of an external operational amplifier that implements the loop filter before the VCO. The Clock Synchronizer delivers this voltage to the two balanced CMOS differential output pins CLK_VCON and CLK_VCOP. These outputs feed the inverting and noninverting inputs of an external operational amplifier that implements the loop filter before the VCO.

Figure 5.3
Clock Recovery Loop



5.5.1 Input Decimation

The CLK_RATIO[2:0] bits (Group 4, APR 18) set the ratio of the VCO clock to the required sample clock in the L64704. For example, if the input signal is 5-Mbaud and the oversampling ratio is $N = 4$, then the input sample frequency is 20 MHz. Under the same conditions, it is possible to use a VCO running at 40 MHz by specifying CLK_RATIO = 1. This corresponds to an input decimation of 2, and in this case every second sample coming from the ADC is fed to the L64704.

This feature allows the satellite decoder control program to choose a reduced VCO range when the L64704 must operate over a wide range of baud rates. Note that setting the CLK_RATIO bits does not switch any decimation filters in the data path; therefore the external IF SAW filtering must fit the baud rate and the oversampling ratio selected via the CLK_DR bits (Group 4, APR 14).

5.5.2 Clock Acquisition and Tracking Modes

The Clock Synchronizer operates in two modes:

- ◆ Clock Acquisition
- ◆ Tracking

5.5.2.1 Clock Acquisition Mode

In the acquisition mode (indicated by CLK_LCF = 0; Group 3, APR 9), the Automatic Frequency Controller (AFC) is active but the Timing Error Detector (TED) is not. Software can disable the AFC after the Clock Synchronizer completes acquisition of the timing loop. This prevents the system from switching back to acquisition mode if a short interrupt occurs during transmission. Setting the CLK_LCF_SUPPRESS bit (Group 4, APR 14) disables the AFC.

The AFC control function determines whether the VCO clock is within the pull-in range of the L64704. If the VCO clock is within the pull-in range, the CLK_LCF bit is set to 1. If the VCO clock is too slow, then the AFC drives a positive voltage on the loop output in order to generate a positive frequency sweep. If the VCO clock is too fast, then the AFC drives a low voltage on the loop output in order to generate a negative frequency sweep.

A counter in the AFC decrements once for each VCO clock edge during the reference period defined below. The microcontroller sets the counter's initial value using the 16-bit CLK_NF register (Group 4, APR 16:17). If the counter has reached either -2, -1, 0, 1, or 2 at the end of the reference period, the VCO clock is within the pull-in range; therefore the AFC sets the CLK_LCF bit to 1 to declare a lock. If the counter value is greater than 3, the VCO clock frequency is too low; therefore the AFC drives a positive voltage on the loop output in order to generate a positive frequency sweep. If the counter value is less than -3, the VCO clock frequency is too high; therefore the AFC drives a low voltage on the loop output in order to generate a negative frequency sweep.

The reference period is determined by the frequency reference from an external crystal. The reference period is derived by preloading a reference counter with the value in the CLK_RP register (Group 4, APR 15). This defines the reference period in multiples of 1024 clock cycles. CLK_RP is a 4-bit register, whose value ranges from 0 to 15.

The external crystal frequency f_{XO} must be less than half the VCO clock frequency f_{VCO} . The recommended value of f_{XO} is 10 MHz and the uncertainty in AFC is:

$$\frac{\pm 2f_{XO}}{(1024 \times \text{CLK_RP})}$$

To ensure that the clock recovery loop locks when the Clock Synchronizer switches from acquisition to tracking mode, the uncertainty in AFC must be lower than the pull-in range of the clock recovery loop.

For CLK_RP = 10 and $f_{XO} = 10$ MHz, the uncertainty is approximately ± 2 kHz. [Equation 5.1](#) relates the parameters described above and must be satisfied for reliable operation.

Equation 5.1

$$f_{VCO} \times (\text{CLK_RP} \times 1024) = f_{XO} \times \text{CLK_NF}$$

For example, consider the following frequency values:

- ◆ Nominal VCO clock frequency, $f_{VCO} = 60$ MHz
- ◆ External crystal frequency, $f_{XO} = 10$ MHz

According to [Equation 5.1](#), CLK_RP and CLK_NF must be set such that:

Equation 5.2
$$60 \times (\text{CLK_RP} \times 1024) = 10 \times \text{CLK_NF}$$

For instance, if you choose CLK_RP = 10 = 0xA, then CLK_NF = 6 x 10 x 1024 = 61440 = 0xF000.

When the VCO clock frequency is within the pull-in range, the Clock Synchronizer closes the clock recovery loop automatically and then enters tracking mode.

5.5.2.2 Tracking Mode

In tracking mode (indicated by CLK_LCF; Group 3, APR 9 = 1), the clock recovery loop is closed and the Sigma Delta ($\Sigma\Delta$) converter takes its input from the Timing Error Detector (TED) output rather than the AFC output.

The loop characteristics are determined by the external active filter with parameters R_{CLK1} , R_{CLK2} , C_{CLK} , and the VCO gain K_{VCO} .

The natural frequency ω_n and the damping factor ζ of the loop are determined by the following formulas:

Equation 5.3
$$R_{CLK2} C_{CLK} = \frac{2\zeta}{\omega_n}$$

Equation 5.4
$$R_{CLK1} C_{CLK} = \frac{1}{\omega_n^2} \times \frac{K_D K_{VCO}}{2\pi M}$$

where M denotes the number of samples per symbol at the ADC and is at least 2, K_D is a constant equal to 1.4 volts, and K_{VCO} is expressed in rad/s/volt. [Table 5.1](#) illustrates how M depends on the value of CLK_DR (Group 4, APR 14) and CLK_RATIO (Group 4, APR 18).

Table 5.1
M as a Function of
CLK_DR and
CLK_RATIO

CLK_DR[1:0]	M
0	$2 \times 2^{\text{CLK_RATIO}}$
1	$4 \times 2^{\text{CLK_RATIO}}$
2	$3 \times 2^{\text{CLK_RATIO}}$

Choose the natural frequency ω_n according to [Table 5.2](#). For fixed rate operation, set the damping factor ζ to one.

Table 5.2
Natural Frequency
as a Function of M

Samples per Symbol, M	Frequency, ω_n (rad/s)
2	3900
3	3178
4	2752
8	1950

For variable rate operation, set ζ to one for the highest oversampling. ω_n decreases for higher oversampling, which corresponds to lower symbol rates.

5.5.3 Output Symbol Clock

The AFC generates an internal symbol clock SCLK, that is used to clock the demodulated symbols DEMI and DEMQ (see [Figure 4.1](#) and [Figure 4.2](#)). This clock can also be brought out on the PCLK pin to clock an external PLL to generate a clock for the decoding pipeline.

5.5.4 Constraints on Data Rates

The I and Q input samples may be 2x, 3x, or 4x oversampled, with a maximum sampling rate of 62.5 Msamples/second.

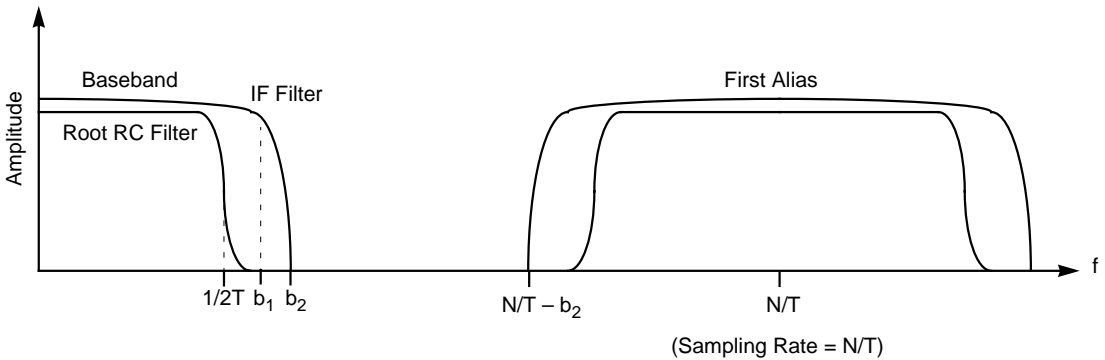
For a given IF SAW filter characteristic and a given oversampling factor N, the range of achievable data rates is limited by two constraints. These constraints are described below and illustrated in [Figure 5.4](#).

1. The signal spectrum must not be distorted by the IF filtering function—that is, the maximum signal frequency must lie within the -1 dB bandwidth ($2b_1$) of the IF SAW filter, as shown in the following equation:

Equation 5.5
$$\frac{(1 + \beta)}{2T} \leq b_1$$

where b is the matched filter roll-off and T is the QPSK (or BPSK) symbol duration.

Figure 5.4
Spectrum of
Oversampled Signal



2. The first alias, centered on the sampling frequency N/T , must not overlap the baseband signal—that is, denoting $2b_2$ as the -30 dB bandwidth of the IF SAW filter.

Equation 5.6
$$\frac{N}{T} - b_2 \geq \frac{(1 + \beta)}{2T}$$

These two constraints together result in the following available baud rate range:

Equation 5.7
$$\frac{2b_2}{2N - (1 + \beta)} \leq \frac{1}{T} \leq \min\left(\frac{2b_1}{1 + \beta}, \frac{f_{max}}{N}\right)$$

where f_{max} is the L64704's maximum operating frequency; 62.5 MHz.

5.5.5 Examples

Consider an off-the-shelf IF SAW filter with cutoff frequencies $b_1 = 16.25$ MHz and $b_2 = 23.8$ MHz. For the roll-off factor $\beta = 0.35$, [Table 5.3](#) shows the range of operational baud rates and data rates for oversampling factors $N = 2, 3$, and 4.

Table 5.3
Example of Data Rates

Oversampling Factor, N	Baud Rate ¹ , 1/T (Mbaud)		Data Rate, R (Mbit/s)	
	Min	Max	Min	Max
2	17.96	24.07	35.92	48.15
3	10.23	20.67	20.46	41.32
4	7.15	15.5	14.3	31

1. The minimum and maximum baud rates delimit an inclusive range.

Table 5.4 shows the achievable data rate ranges for a narrower off-the-shelf IF SAW filter with $b_1 = 11.9$ MHz, $b_2 = 16.25$ MHz, and $\beta = 0.35$.

Table 5.4
Example of Data Rates for Narrow SAW Filter

Oversampling Factor, N	Baud Rate ¹ , 1/T (Mbaud)		Data Rate, R (Mbit/s)	
	Min	Max	Min	Max
2	12.26	17.63	24.52	35.25
3	6.99	17.63	13.98	35.26
4	4.89	15.55	9.77	31.1

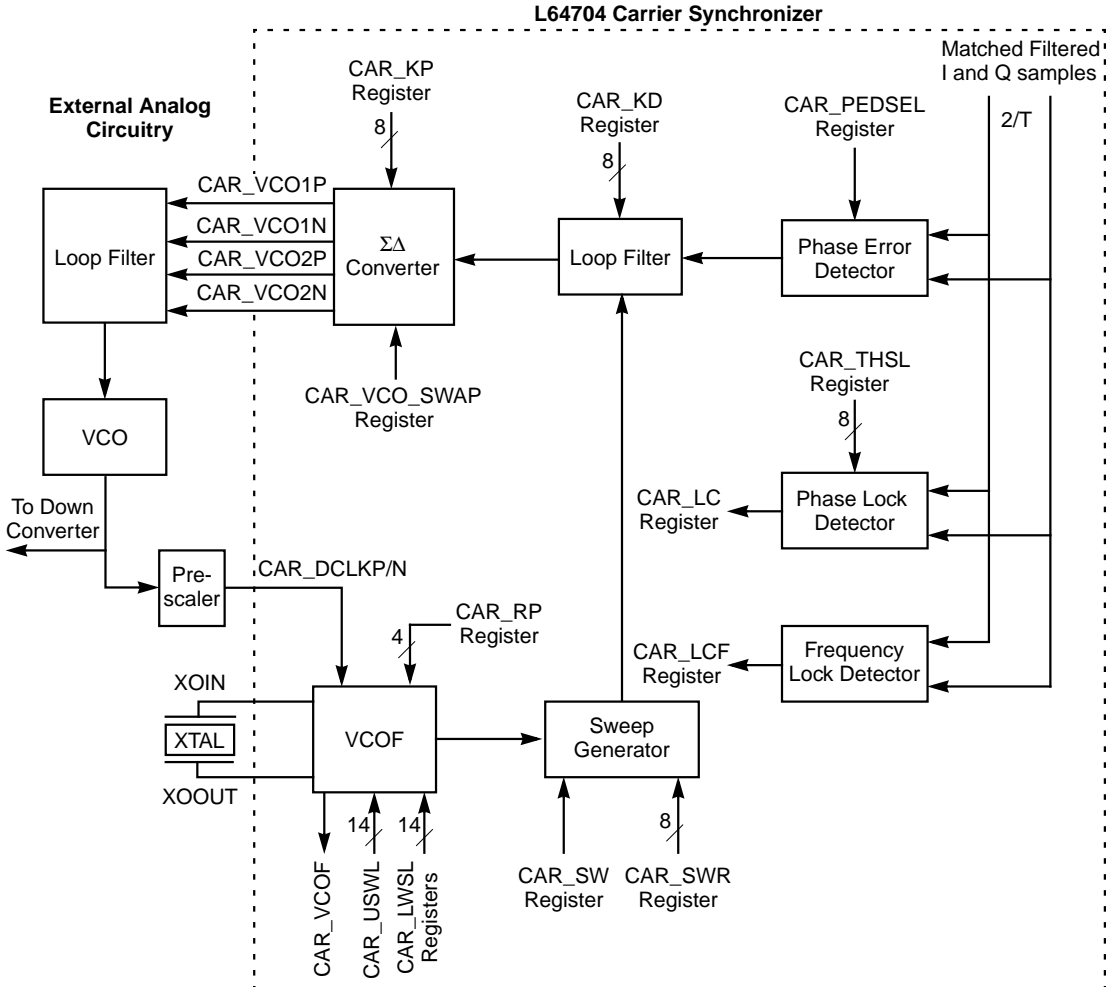
1. The minimum and maximum baud rates delimit an inclusive range.

5.6 Carrier Synchronizer

Figure 5.5 illustrates the Carrier Synchronizer. This circuit consists of the following functional elements:

- ◆ A phase error detector
- ◆ A digital loop filter
- ◆ A phase lock detector
- ◆ A frequency sweep generator
- ◆ A frequency lock detector

Figure 5.5
Carrier Recovery Loop



Because the outputs of off-the-shelf tuners for DVB satellite receivers have a large frequency uncertainty (a common order of magnitude is ± 5 MHz), the L64704's Carrier Synchronizer includes a frequency sweep generator for signal acquisition.

To minimize the complexity of external analog circuitry for the loop filter, the L64704 implements part of the loop filter digitally. The external part of the loop filter consists of only fixed components. You can choose values for these components that cover a whole range of data rates.

The Carrier Synchronizer provides its output to the analog filter through two $\Sigma\Delta$ differential pairs; CAR_VCO1P/N and CAR_VCO2P/N. Depending on the value of the CAR_VCO1N/P and CAR_VCO2N/P bits (Group 4, APR 33), the Carrier Synchronizer selects one pair and 3-states the other pair. An analog integrator adds the signals together externally, where the signals of pair 2 are weighted with a different factor relative to the signals of pair 1. You choose different values for R_{CAR1} and R_{CAR2} to change the weighting factor (see [Section 5.6.2.2, “Loop Characteristics”](#)). This feature provides a means for adjusting the loop bandwidth over a larger range than would be possible with pure $\Sigma\Delta$ modulation.

5.6.1 Carrier Acquisition

During carrier acquisition, the internal frequency sweep generator searches for the correct frequency. To vary the sweep rate, change the value in the CAR_SWR register (Group 4, APR 28); to start the sweep generator, set the CAR_SW bit (Group 4, APR 33) to 1.

5.6.1.1 Frequency Sweep Limits

The CAR_USWL (Group 4, APR 29:30) and CAR_LSWL (Group 4, APR 31:32) registers set the upper and lower limits, respectively, of the frequency sweep.

The frequency sweep uses an external crystal that produces a reference clock (the same crystal as for clock acquisition). See [Appendix C, “Oscillator Cells”](#) for details.

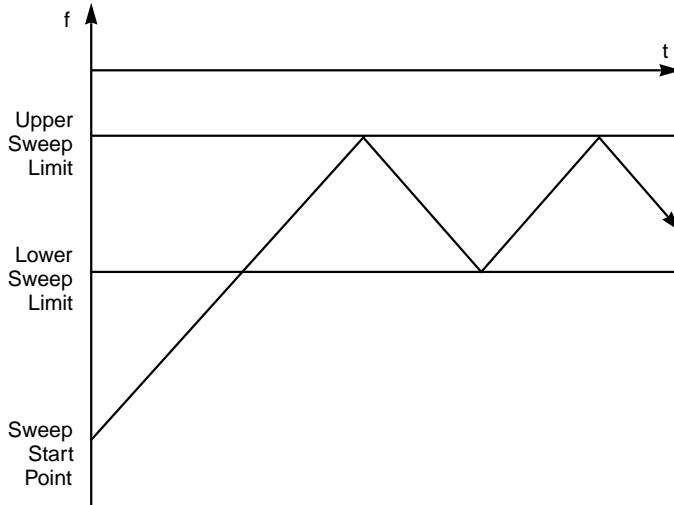
The external prescaler divides the frequency of the carrier VCO by a constant number (32, for example) and then feeds it into the L64704 on the CAR_DCLK pair of differential input pins. You should design the prescaler so that the frequency is faster than the crystal reference frequency and slower than 80% of the CLK frequency.

The reference period for the VCO frequency measurement ends when a decrementing reference counter driven by the reference clock reaches zero. The L64704 loads the counter with the value in the 4-bit CAR_RP register (Group 4, APR 24). This value defines the reference period in multiples of 1024 clock cycles.

The prescaled clock drives an incrementing counter within the VCOF block that is reset at the beginning of the reference period. The VCOF logic then checks the value of the counter at the end of the reference period. If the prescaled frequency is below the lower limit set in the

CAR_LWSL register (Group 4, APR 31:32), the VCOF block automatically tells the sweep generator to increase the VCO frequency. If the prescaled frequency is above the upper limit set in the CAR_USWL register, the VCOF block tells the sweep generator to decrease the VCO frequency. Figure 5.6 illustrates how the sweep generator keeps the VCO frequency within the established limits.

Figure 5.6
Frequency
Sweeping



For example, consider the following frequency values:

- ◆ VCO nominal frequency = 480 MHz
- ◆ Frequency uncertainty = ± 3 MHz
- ◆ prescaling ratio = 32

With these values, the lower prescaled frequency is $(480 - 3)/32 = 14.90625$ MHz, and the upper prescaled frequency is $(480 + 3)/32 = 15.09375$ MHz.

If the CAR_RP register is set to 8, the reference period is 8192 reference clock cycles (for instance, at 10 MHz), and the upper and lower sweep limits must have the following values:

$$\text{CAR_LSWL} = 14.90625 \times \frac{8192}{10} = 12,211 \text{ (lower limit)}$$

$$\text{CAR_USWL} = 15.09375 \times \frac{8192}{10} = 12,365 \text{ (upper limit)}$$

5.6.1.2 Carrier VCO Frequency Measurement

The L64704 puts the result of the VCO frequency measurement into the 16-bit CAR_VCOF register (Group 3, APR 6:7) for the microcontroller to read. You must read both nibbles before the L64704 releases this register for a new value.

The L64704 computes the value that it puts into the CAR_VCOF register based on [Equation 5.8](#).

Equation 5.8

$$\text{CAR_VCOF} \times f_{x0} = \text{CAR_RP} \times 1024 \times \frac{f_{\text{CAR_VCO}}}{\text{prescaler}}$$

For example, if $f_{x0} = 10$ MHz, $\text{CAR_RP} = 8$, $f_{\text{CAR_VCO}} = 480$ MHz, and $\text{prescaler} = 32$, then

$$\text{CAR_VCOF} = \frac{f_{\text{CAR_VCO}} \times \text{CAR_RP} \times 1024}{f_{x0}} = \frac{480 \times 8 \times 1024}{10 \times 32} = 12288$$

So that the value each bit in the CAR_VCOF register is given by the following:

$$\frac{f_{\text{CAR_VCO}}}{\text{CAR_VCOF}} = \frac{480 \times 10^6}{12288} = 39062 \text{ Hz}$$

Therefore if $\text{prescaler} = 16$, then the value for each bit in the CAR_VCOF register is 14.5 kHz.

5.6.1.3 Frequency Sweep Without Prescaled Frequency Signal

The frequency sweep generator can also operate without using the prescaled frequency. This can be very convenient if the analog front end does not provide for a prescaler function.

In this case, both the CAR_USWL (Group 4, APR 29:30) and CAR_LSWL (Group 4, APR 31:32) registers must be set to zero. The state of the CAR_SWP_SWP (Group 4, APR 33) bit controls the sweep direction. Even though the Carrier Synchronizer controls the frequency sweep rate based on the value in the CAR_SWR register (Group 4, APR 28), the microcontroller must monitor the sweep direction itself.

5.6.1.4 Frequency Sweep Rate

The Carrier Synchronizer determines the frequency sweep rate based on the value in the CAR_SWR register. Set the value in the 8-bit CAR_SWR register based on [Equation 5.9](#).

Equation 5.9
$$\text{CAR_SWR} = 64K_D\theta_\infty$$

K_D is the gain of the carrier phase error detector. Assuming a standard power reference value (the value in the PWR_REF register, Group 4, APR 19, is 84), K_D has a typical value of 10 for low Eb/No conditions (4 dB) for both the DDML and the NDAML phase error detectors (see [Section 5.6.2, "Carrier Phase Tracking"](#)). For larger Eb/No conditions (10 dB), K_D is around 26 for the DDML and around 42 for the NDAML.

K_D grows linearly with $\sqrt{\text{PWR_REF}}$. θ_∞ is the phase loop steady state error during acquisition. It should always remain lower than 5 degrees. During the tracking phase, the loop drives the residual steady state error to 0.

[Equation 5.10](#) gives the sweep rate in Hertz per second.

Equation 5.10
$$\dot{f} = \text{CAR_SWR} \cdot \frac{3.3}{128\pi} \cdot \frac{K_{VCO}}{R_{CAR}C_{CAR}(\text{CAR_KP})}$$

For example, if $K_D = 10$ and $\theta_\infty = 3^\circ = 0.052 \text{ rad}$, then $\text{CAR_SWR} = 33$. Assuming the analog components verify [Equation 5.11](#), and CAR_KP (Group 4, APR 25) = 50, we get $df/dt = 32.6 \text{ MHz per second}$.

5.6.1.5 Phase Lock Detection

Once the VCO frequency is close enough to the frequency of the incoming wave, the signal lies in the pull-in range of the phase-locked loop. When the loop is phase locked, the phase lock detector sets the CAR_LC bit (Group 3, APR 9) to 1. To stop the sweep, the microcontroller must then set the CAR_SW bit (Group 4, APR 33) to zero.

The phase lock detector uses an internal threshold and an estimation period, which are programmable using the CAR_THSL register (Group 4, APR 27) and the CAR_OUT_SEL bit (Group 4, APR 33), respectively.

The CAR_OUT_SEL bit selects between a long and a short estimation period. For operation at low Eb/No (less than 10 dB), the long period should be selected (CAR_OUT_SEL = 0). A typical value of CAR_THSL is then 31.

For operation at higher Eb/No (10 dB or higher), the short period can be selected. This provides for a faster lock detection. In this case, a typical value for CAR_THSL is 72.

5.6.1.6 Frequency Lock Detection

The frequency lock detector also has a configurable estimation period, selectable by the same parameter as for phase lock detection (the CAR_OUT_SEL bit). No threshold values have to be programmed for the frequency lock detector; the thresholds are fixed and hard-coded in the L64704.

5.6.1.7 False Locks

The microcontroller must take particular care to handle a false lock condition correctly. A false lock occurs when phase lock has been detected but the correct central frequency has not been reached yet. This situation happens in QPSK for frequency offsets that are multiples of $1/4T$, where T is the QPSK symbol duration.

This case is detected by CAR_LC = 1 and CAR_LCF = 0 (both bits are in Group 3, APR 9). When the microcontroller detects this situation, it should set the CAR_OPEN (Group 4, APR 33) bit to 1 and reset it after CAR_LC = 0. This has the effect of opening the carrier loop, forcing the loop to run out of the false lock point.

5.6.2 Carrier Phase Tracking

5.6.2.1 Phase Error Estimator

In QPSK mode ($CON_SEL = 0$; Group 4, APR 35), the phase error detector implements two error estimators:

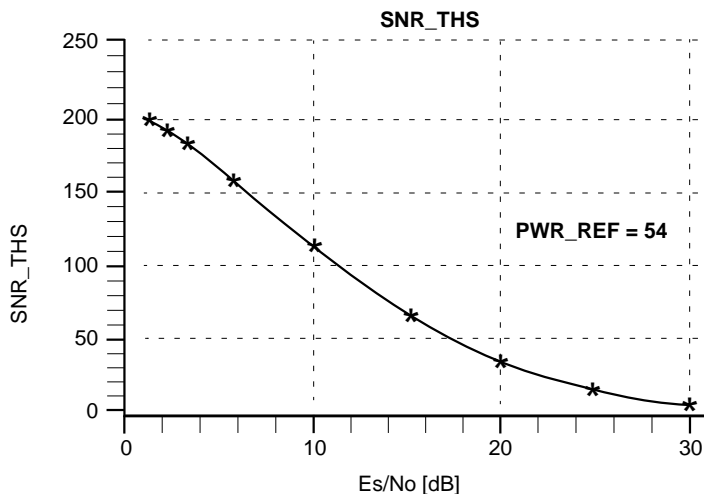
- ◆ a Non-data Aided Maximum Likelihood (NDAML) estimator
- ◆ a Decision Directed Maximum Likelihood (DDML) estimator

The microcontroller selects the estimator via the CAR_PED_SEL bit (Group 4, APR 33). $CAR_PED_SEL = 0$ sets the DDML estimator; $CAR_PED_SEL = 1$ sets the NDAML estimator.

In BPSK mode ($CON_SEL = 1$), the phase error detector implements a single DDML estimator.

The phase detector uses two gain values depending on the signal to noise ratio. The SNR is internally estimated and compared to an 8-bit threshold; SNR_THS (Group 4, APR 22). The plot in [Figure 5.7](#) shows the relation between the SNR_THS parameter and the actual Es/No (symbol energy to noise power density) seen in the circuit. The value $SNR_THS = 100$ corresponding to an actual $Es/No = 11$ dB is recommended. The result of the comparison of the estimated SNR to the threshold is stored in the $Demod_SNR$ bit (Group 3, APR 6, bit 7).

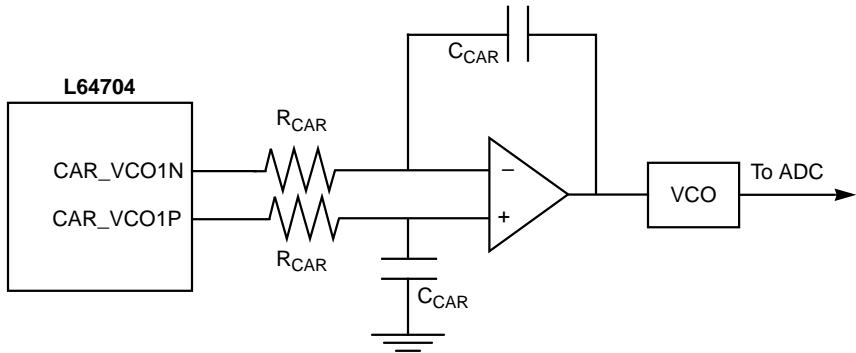
Figure 5.7
SNR Threshold vs.
 Es/No



5.6.2.2 Loop Characteristics

To set the parameters of the carrier recovery loop (natural frequency and damping factor), you must select both the values the microcontroller writes into the registers CAR_KD (Group 4, APR 26) and CAR_KP (Group 4, APR 25), and the values of the resistors and capacitors of the external active filter (shown in [Figure 5.8](#)).

Figure 5.8
Carrier Loop Filter
Schematic



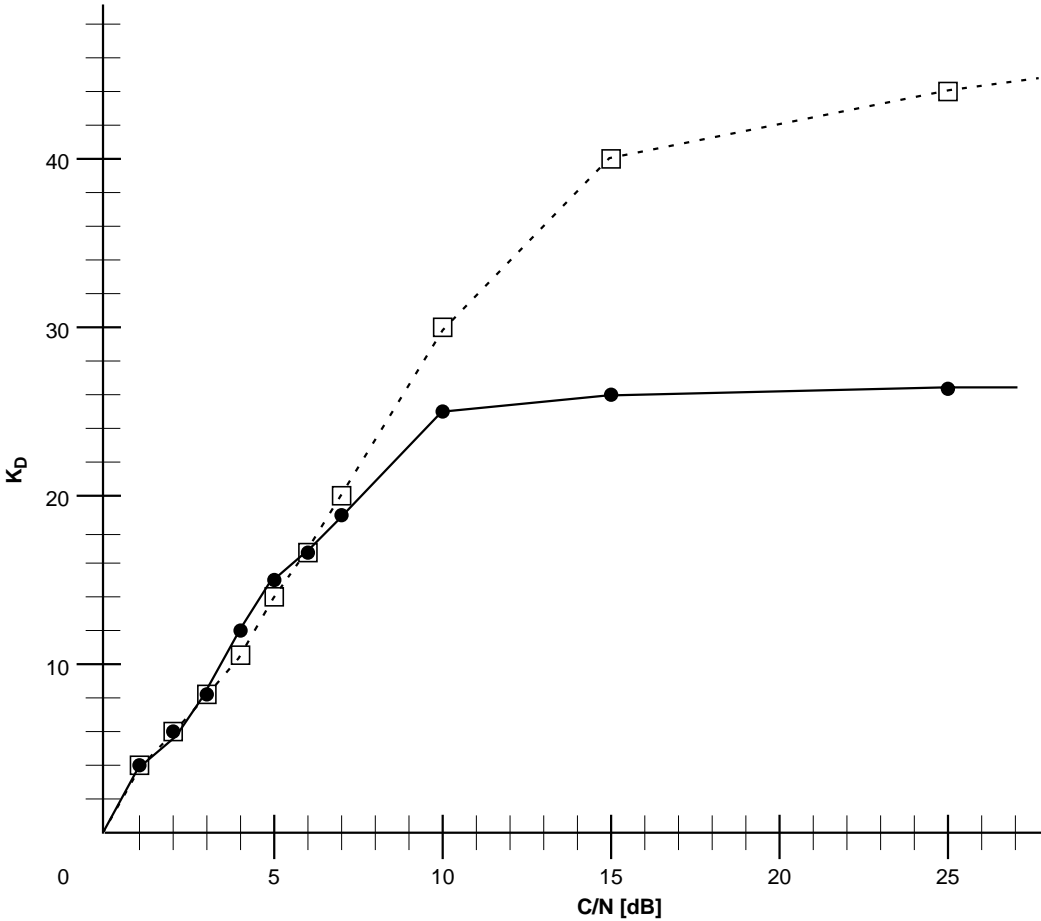
The natural frequency ω_n (rad/s) and the damping factor ζ of the loop are determined by the following equations.

Equation 5.11

$$\zeta = 2 \cdot \text{CAR_KD} \cdot \omega_n \cdot T, \quad \omega_n = \sqrt{\frac{3.3K_D K_{\text{CARVCO}}}{R_{\text{CAR}} C_{\text{CAR}} (\text{CAR_KP})}}$$

K_D is the Phase Detector Gain and it depends on whether DDML or NDAML is selected. [Figure 5.9](#) presents the gains of the two phase detectors as a function of the Carrier to Noise ratio (C/N).

Figure 5.9
PED Slope



Key:

—●—	DDML
- - -□-	NDAML

K_D is about 10 for $C/N = 4$ dB (Channel $E_s/N_o = 1$ dB).

Set $K_D = 10$, $K_{CARVCO} = 1.8$ MHz/V = 11.3 Mrad/s/V and $\omega_n = 32$ K rad/s/v.

T represents the QPSK symbol duration. Twice the value of the parameter CAR_KP determines the resolution of the $\Sigma\Delta$ conversion; it should be kept above 30 and below 127 for 6 bits of resolution.

The loop filter output is provided with two $\Sigma\Delta$ modulated complementary signal pairs, CAR_VCO1P and CAR_VCO1N, and AR_VCO2P and CAR_VCO2N. These signals connect to the external active integrator, that completes the loop filter chain (Figure 5.8). One of the complementary pairs is selected while the other is 3-stated, depending on the settings of the CAR_VCO1N/P and CAR_VCO2N/P bits (Group 4, APR 33). After reset, both complementary pairs are active. Externally, these signals are added together in the analog integrator. The CAR_VCO2P/N outputs should be weighted with a different factor with respect to the CAR_VCO1P/N outputs by proper selection of the corresponding resistors and capacitors. With two pairs of loop-filter outputs, you can adjust the loop bandwidth over a large range of data rates by enabling one or the other of the output pairs.

5.6.2.3 Low Baud Rate Operation

For low-baud-rate operation (between one and five Mbaud), the Sigma-Delta conversion used in the carrier loop introduces a delay that makes the carrier loop too narrow for reliable operation.

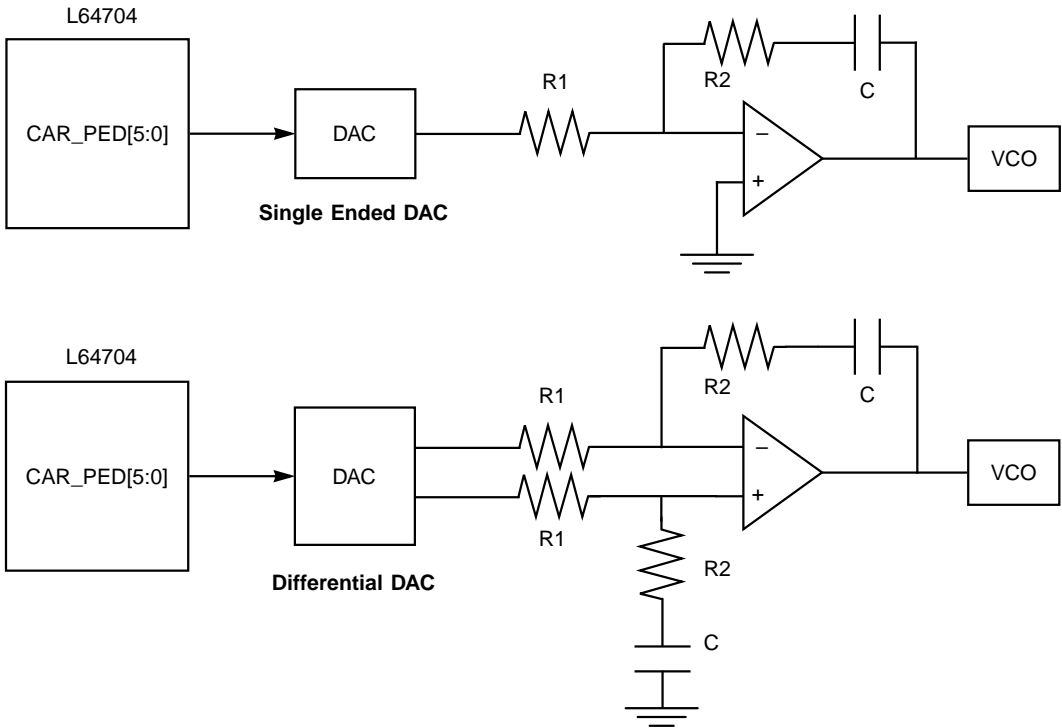
For this type of application, program the CAR_OUT_SEL bit (Group 4, APR 33) so that the L64704 Carrier Loop pins carry the Phase Error Detector to DAC (CAR_PED[5:0]) outputs instead of the CAR_VCOxP/N outputs. The CAR_PED signal is simply the digital signal before Sigma-Delta conversion. It is intended to be connected to an external 6-bit DAC, that then feeds a similar active low-pass filter as described previously. You program the L64704 to output the SCLK signal on the DVALIDOUT pin by setting the SYNC/SCLK bit (Group 4, APR 14) to 1. The SCLK signal on the DVALIDOUT pin is used to clock the external DAC.

You should set the CAR_PED_SEL bit to 1 to enable the CAR_PED[5:0] outputs. You also need to feed the voltage level from the DAC's output to a loop filter similar to one of the filters shown in Figure 5.10.

For low bit rate applications that use an external DAC, you must enable both Sigma-Delta outputs by setting Carrier Loop Configuration Register (Group 4, APR 33) bits [5:4] to zero.

The output of the DAC interface, CAR_PED[5:0] is in offset binary format. A value of '000000' produces a decrease in the VCO control voltage. A value of '111111' produces an increase in the VCO control voltage. The value '100000' is the zero control voltage.

Figure 5.10
Using CAR_PED
Outputs



1. Choose CAR_KD as described in [Section 5.6.1.4](#), “Frequency Sweep Rate.”
2. Choose ζ (see [Equation 5.11](#)).
3. Choose ω_n (see [Equation 5.11](#)).
4. Calculate R_2 , R_1 , and C from the following equations:

$$\frac{R_2 \cdot C \cdot \omega_n}{2}, \omega_n = \sqrt{\frac{K_D K_{carvco}(\text{CAR_KD}) \text{ADR}}{R_1 C \times 8192}}$$

ADR is one side of the DAC range. For example, if the DAC output range is ± 1 volt, then ADR = one.

5.7 Automatic Gain Control (AGC)

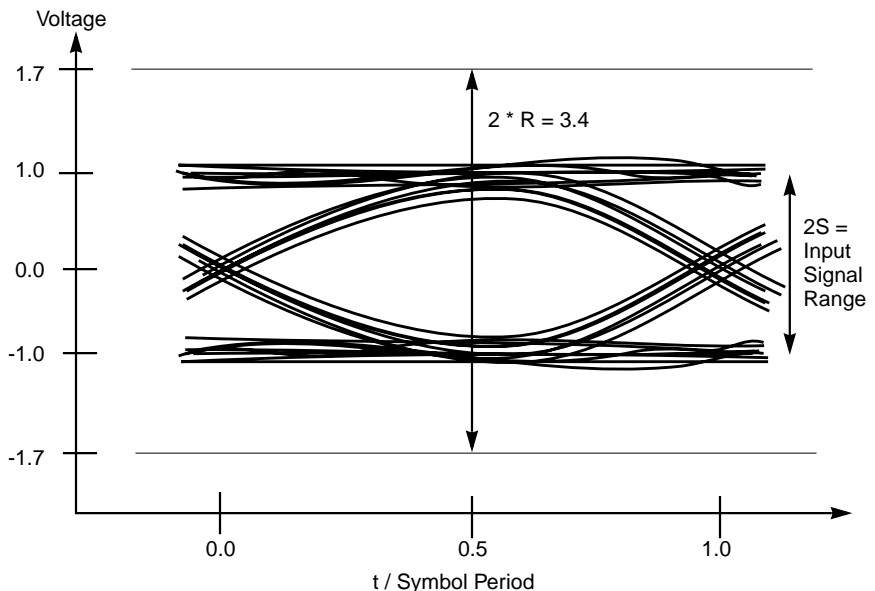
This section describes the L64704's automatic gain control (AGC) and is divided into the following subsections:

- ◆ [Section 5.7.1, "ADC Range and Power Reference"](#)
- ◆ [Section 5.7.2, "Power Control Loop"](#)
- ◆ [Section 5.7.3, "Power Level"](#)

5.7.1 ADC Range and Power Reference

When the PWR_REF register (Group 4, APR 19) is set to the recommended value of 84, the AGC sets the ratio of the signal range to the Analog-to-Digital Converter (ADC) range to 1:1.7 (see [Figure 5.11](#)).

Figure 5.11
Eye Pattern and
ADC Range



Assuming that the signal power at the input of the ADC is normalized to $1 V^2$, the range of the signal ($2S$) is 2 V (the noise-free level of the I and Q signals). The value of PWR_REF is computed from [Equation 5.12](#).

Equation 5.12
$$PWR_REF = \frac{243 \cdot L}{R^2}$$

where $L = 1$ if CLK_DR (Group 4, APR 14) = 0 (no internal decimation filter is used), or $L = 4$ if CLK_DR = 1 or 2. R is the ADC range. For $L = 1$

and a unit signal level, a recommended value for R is 1.7, which corresponds to $PWR_REF = 84$. For $L = 4$, a recommended value for R is 3.4, which also corresponds to $PWR_REF = 84$.

The ratio of the signal level to the ADC range is constant ($S:R = 1:1.7$) in [Figure 5.11](#). If the ADC range changes, the AGC scales the signal level to keep the $S:R$ ratio constant.

5.7.2 Power Control Loop

The L64704 measures the signal power at the output of the matched filter and compares the measured value to an expected value that the microcontroller has written into the PWR_REF register.

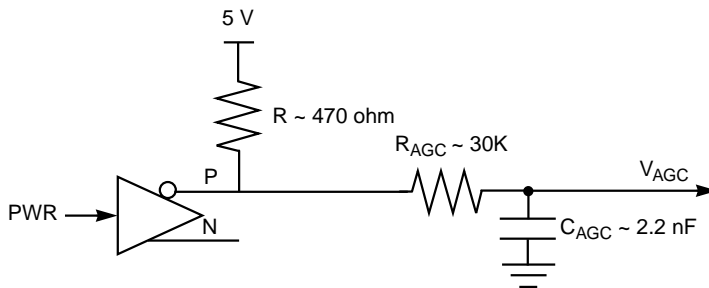
The microcontroller can adjust the power loop bandwidth using the $PWR_BW[1:0]$ bits (Group 4, APR 20). The loop bandwidth is proportional to PWR_BW and proportional to the symbol rate. Set the PWR_BW bits according to [Table 5.5](#).

Table 5.5
 PWR_BW as a Function of Symbol Rate

PWR_BW	Symbol Rate (MHz)
0	20 - 45
1	10 - 20
2	5 - 10
3	2 - 5

The power control signal drives the $\Sigma\Delta$ modulated output $PWRP$. You use this output to drive an external passive RC filter that feeds the gain control stage ([Figure 5.12](#)).

Figure 5.12
AGC Loop Control



The R and C values for the passive low-pass filter should be such that $R_{AGC}C_{AGC} \cong 64 \mu s$.

5.7.3 Power Level

The L64704 stores the AGC loop control voltage in the PWR_LVL[7:0] register (Group 3, APR 8), where the microcontroller can monitor it. The relation between the loop voltage V_{AGC} and the PWR_LVL register is:

$$V_{AGC} = \frac{\text{PWR_LVL}}{256} \times V_{REF}$$

The PWRP pin uses an open drain buffer that allows you to apply an external V_{REF} voltage of 5 V even if the L64704 is powered at 3.3 V.

5.8 Output Control

Because the output of the matched filter is quantized to three bits for the subsequent Viterbi decoder, the L64704's Output Control properly adjusts the level of the output signals.

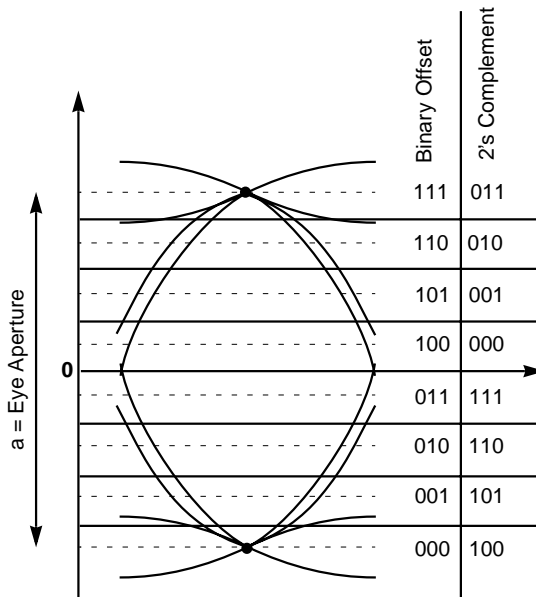
The microcontroller can adjust the level of the demodulated DEMI and DEMQ output signals using the SCALE register (Group 4, APR 21). The SCALE register multiplies the results of the matched filter before it is truncated to the 3-bit outputs.

When the PWR_REF register (Group 4, APR 19) is set to its recommended value of 84, SCALE[7:0] should be set to 158. In this case, the spacing for the 3-bit quantized outputs DEMI and DEMQ is equal to $a/8$, where a is the eye amplitude of the noise free matched filter output. Refer to [Figure 5.13](#).

SCALE[7:0] should be set according to the following table:

Viterbi Rate			Scale
1/2	2/3	3/4	158
	5/6	7/8	190

Figure 5.13
Eye Pattern and
Soft Decision
Thresholds



The useful part of the matched filter output signal is clipped for a larger value of SCALE.

Because the power control loop automatically reduces the eye amplitude for increasing noise, the DEMI and DEMQ signals include additional headroom for resolving noise.

Equation 5.13 relates SCALE and PWR_REF.

Equation 5.13
$$\text{SCALE} \times \sqrt{2 \times \text{PWR_REF}} = 2047$$

5.9 Other Functions

The following functions have been added in order to simplify the design of the analog front end, to reduce the amount of external circuitry, and to make the board layout as simple as possible.

5.9.1 Carrier Loop DC Offset Compensation

As discussed in previous sections, filtering in the carrier loop is carried out in the analog domain. Because of the imperfections of analog components, the loop voltage could show a DC offset. This would have two consequences:

- ◆ During the acquisition phase, the frequency sweep becomes asymmetric. The DC offset slows down the sweep in one direction and makes it faster in the other direction. If the sweep is too slow, false locks can occur at high SNR. If the sweep is too fast, locks can be missed at low SNR.
- ◆ During the tracking phase, the static error of the loop is not minimum. This is because the DC offset generates a frequency ramp that the loop has to compensate for.

For these reasons, the L64704 implements an internal offset compensation in the carrier loop. This internal compensation operates in two modes: acquisition and tracking.

5.9.1.1 Carrier Acquisition Phase

In the acquisition phase, the L64704 reads the DC offset estimation from the CAR_OFFSET[7:0] register (Group 4, APR 15) and subtracts it from the loop voltage. The CAR_OFFSET register is assumed to have been previously loaded by the microcontroller. The CAR_OFFSET parameter is a signed integer ranging from -128 to +127.

- ◆ T_{up} can be measured by using an oscilloscope.
- ◆ If T_{up} is the ramp-up time and T_{down} the ramp-down time (with CAR_OFFSET = 0 and CAR_OPEN = 1, open loop), then the CAR_OFFSET value can be computed by the following formula:

Equation 5.14

$$CAR_OFFSET = \pm \frac{CAR_SWRT}{2} \frac{T_{down} - T_{up}}{T_{down} + T_{up}}$$

The \pm choice depends on the polarity of the N/P outputs. Select + if polarity is normal; select - if it is swapped.

5.9.1.2 Carrier Tracking Phase

In the tracking phase, the mean value of the phase error should be zero. The mean value is internally computed and subtracted from the phase error before Sigma-Delta conversion. This estimation and subtraction system is only enabled in tracking mode, that is, when `CAR_SW = 0`.

The maximum offset voltage that can be compensated for by this mechanism is shown in [Equation 5.15](#).

Equation 5.15

$$V_{offmax} = \frac{CAR_OFFSET}{32} \frac{3.3V}{CAR_KP}$$

Note the following examples:

- ◆ for `CAR_KP = 255`, $V_{offmax} = 51$ mV (resolution 0.4 mV)
- ◆ for `CAR_KP = 30`, $V_{offmax} = 436$ mV (resolution 3.4 mV)

5.9.2 External Controls

Five external control bits are available on the L64704. Four of these bits are output signals, and one is an input signal. These controls can be used to set up or to read parameters from other components on the board (like the RF front end and the tuner) using only the microcontroller interface of the L64704.

The four output controls use pins `XCTR_OUT.0`, `XCTR_OUT.1`, `XCTR_OUT.2`, `XCTR_OUT.3`. They are programmed by setting their respective bits in the `XCTR[3:0]` register (Group 4, APR 36). The `XCTR[i]` register drives the `XCTR_OUT.i` pin; that is, programming the `XCTR[i]` register to 0 sets a 0 volt level on pin `XCTR_OUT.i`, and programming the `XCTR[i]` register to 1 sets a 3.3 volt level on pin `XCTR_OUT.i`.

The input control is sensed on the `XCTR_IN` pin. The logic level applied to this pin is read using the `XCTR_IN` bit (Group 3, APR 6).

5.9.3 Hi-Z Mode on Functional Outputs

When `F_OUT_HiZ` is set to 1, all the functional outputs of the L64704 are set to the high-impedance mode. These outputs include `CLK_VCON/P`, `CAR_VCOxN/P` and `PWRP`.

Chapter 6

Decoding Pipeline Synchronization

This chapter describes the configurable synchronization circuit that aligns the decoding pipeline outputs to the overall frame structure of the L64704. The decoding pipeline consists of the Viterbi Decoder, Deinterleaver, Reed-Solomon (RS) Decoder, and the Descrambler. This chapter consists of four sections:

- ◆ [Section 6.1, “Synchronization Scheme,”](#) provides an overview of the Decoding Pipeline three stage synchronization process.
- ◆ [Section 6.2, “Viterbi Decoder Synchronization,”](#) describes the synchronization module for the Viterbi Decoder.
- ◆ [Section 6.3, “Reed-Solomon Deinterleaver Synchronization,”](#) shows the synchronization process for the Reed-Solomon Deinterleaver.
- ◆ [Section 6.4, “Descrambler Synchronization,”](#) describes the synchronization module for the Descrambler module.

6.1 Synchronization Scheme

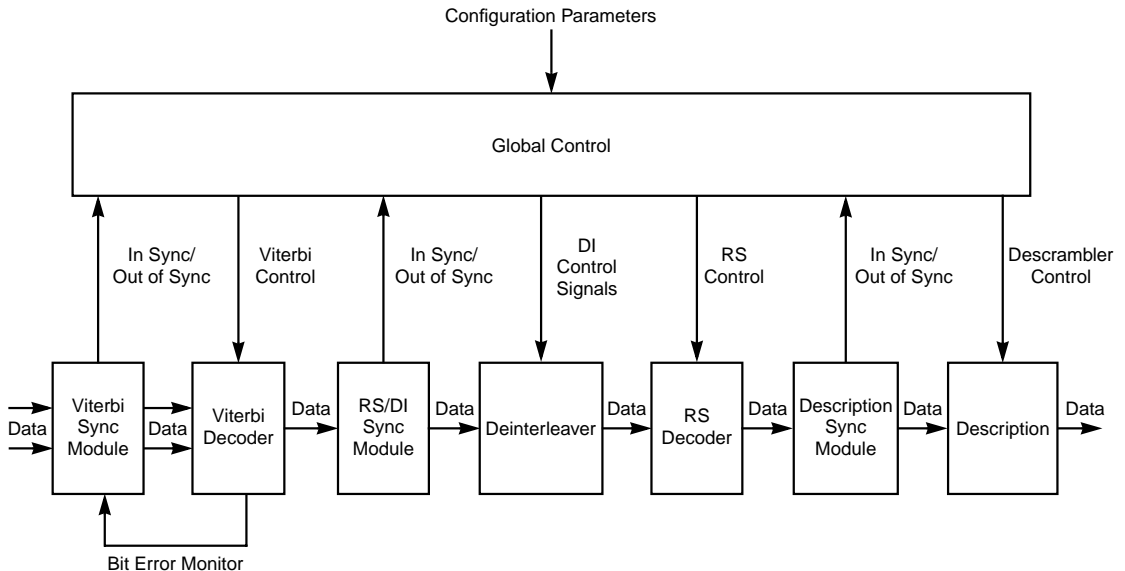
The L64704's FEC synchronization scheme is composed of a three stage synchronization process:

- ◆ The first stage synchronization uses output statistics from the Viterbi Decoder module.
- ◆ The second stage identifies a synchronization word.
- ◆ The third stage identifies an inverting synchronization word.

A global control module generates the control signals for the Viterbi, Descrambler, Deinterleaver, and RS Decoder modules. The global control module handles the appropriate sequencing of the synchronization signals for determining in- and out-of-synchronization. The input to the FEC portion of the L64704 is two three-bit symbols generated by the demodulator portion. The maximum information rate is 62.5 Mbits/s.

Figure 6.1 shows the position of and major connections to the synchronization module.

Figure 6.1
Synchronization
Module

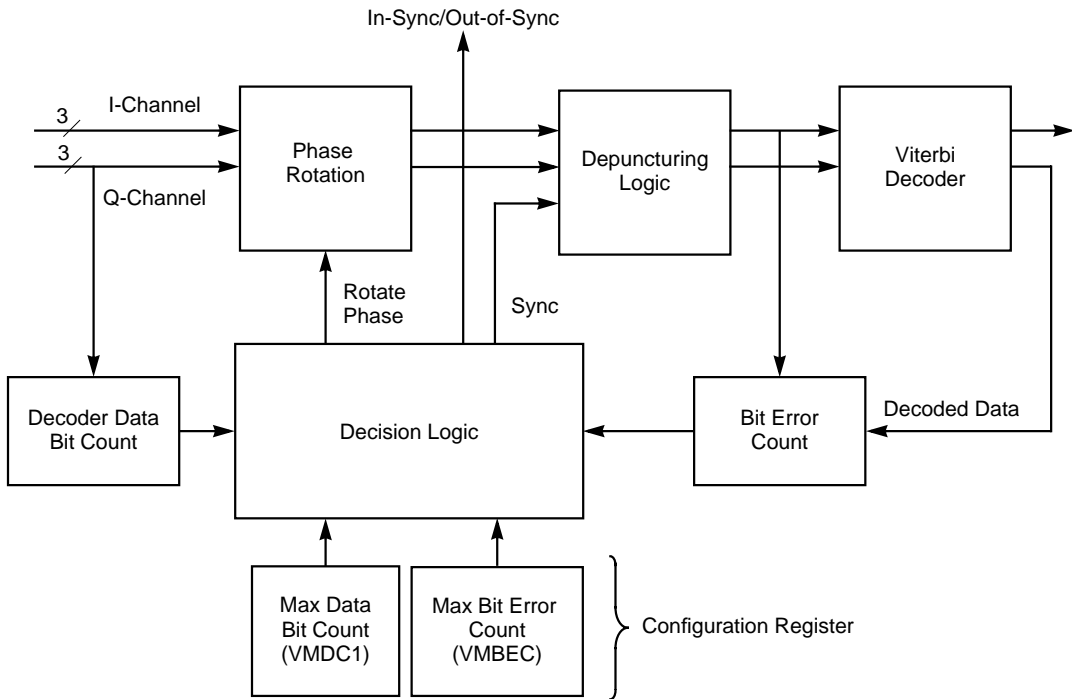


6.2 Viterbi Decoder Synchronization

This section describes the first stage, or Viterbi Decoder synchronization. Figure 6.2 illustrates the Viterbi Decoder synchronization process.

In the first stage, the decoder observes the valid data symbols and bit errors in the decoded data stream to determine the in- or out-of-synchronization condition. The Viterbi Max Data Bit Count Registers (VMDC1; Group 4, APR 4, and VMDC2; Group 4, APR 5:7) set the number of valid data bits at the output of the Viterbi Decoder over which the decoder counts channel symbol errors. During that interval, whenever the bit error count is above the value specified in the Viterbi Max Data Bit Error Count Register (Group 4, APR 8), the synchronization logic flags an out-of-synchronization condition.

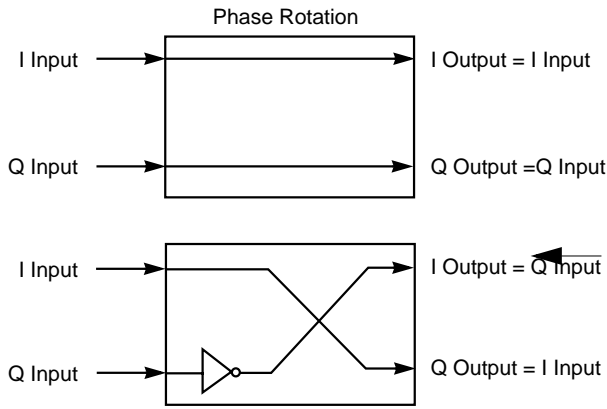
Figure 6.2
Viterbi Decoder
Synchronization



The decoder then proceeds to adjust either the phase in the phase rotation module or the data stream alignment in the depuncturing logic by successively stepping through as many combinations as needed (and possibly all combinations) until synchronization is achieved. Because both I and Q channels can appear inverted and swapped, four phases are possible for the phase rotation block. Depending on the Viterbi code rate chosen, the depuncturing mechanism includes up to two states. (The 180 degree rotation is removed in the Reed-Solomon decoder)

synchronization stage. See [page 6-10.](#)) [Figure 6.3](#) outlines the operations performed during phase rotation:

Figure 6.3
Phase Rotation for
Synchronization



A misaligned data stream results in a difference in the bit error rate at the Viterbi Decoder output, compared to that of the original message, of about 0.5. The mechanism implemented provides strong correlation between an out-of-sync condition and the observed bit error rate.

This first synchronization stage does not inspect the data stream for specific synchronization patterns, nor does it remove any portions of the data stream. Once the Viterbi Decoder module has reached synchronization, the following blocks in the data pipeline (the Deinterleaver and Reed-Solomon Decoder) each require their own synchronization procedures.

6.3
Reed-Solomon
Deinterleaver
Synchronization

This section describes the second synchronization stage; Reed-Solomon Deinterleaver synchronization. In the second synchronization stage, the decoder searches the data stream for a pre-defined sync word to determine the in-sync or out-of-sync condition. Figure 6.4 illustrates the Reed-Solomon Deinterleaver synchronization process.

Figure 6.4
Reed-Solomon,
Deinterleaver
Synchronization

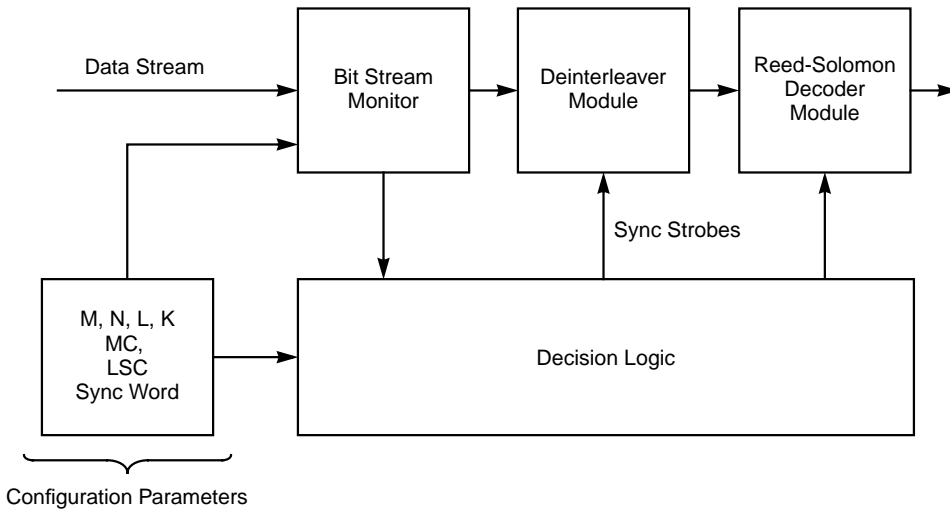
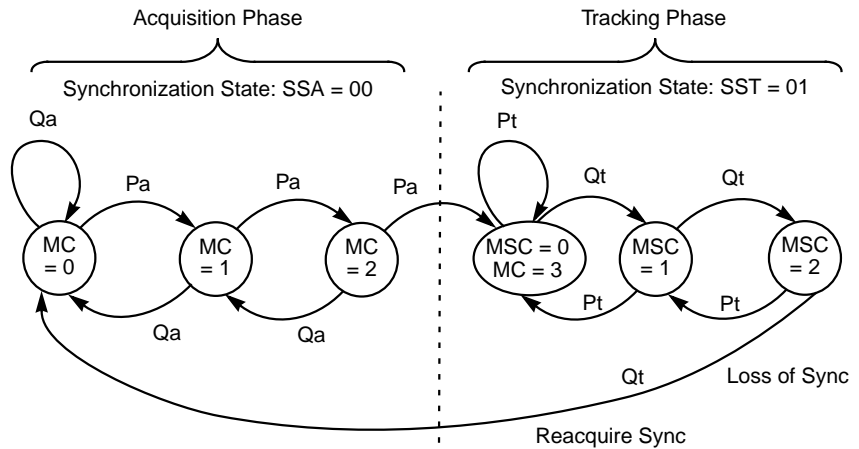


Figure 6.5 shows an example state diagram that outlines how the decoder determines synchronization, tracking, and loss of synchronization in this stage.

Figure 6.5
Synchronization,
Tracking, and Loss
of Sync for 3
Missed Sync
Words



Pa: State Transition, Sync Word Detected (N, M, K)

Qa: State Transition, Sync Word Misdetected

Pt: State Transition, Sync Word Detected (N, M, L)

Qt: State Transition, Sync Word Not Detected

The parameters in [Figure 6.5](#) are defined as follows:

- N** Length of the RS codeword in bytes
- M** Length of synchronization word in bits ($M = 8$, fixed)
- K** The maximum number of mismatching bits allowed to declare a match when comparing M bits in the data stream to the reference sync word during acquisition phase ($K = 0$, fixed)
- MC** Match Counter, number of sync word matches found so far during acquisition phase
- L** Maximum number of mismatching bits allowed to declare a match when comparing M bits in the data stream to the reference sync word during tracking phase ($L = 0, 1, \text{ or } 2$)
- MSC** Mismatch Counter, number of sync word mismatches found so far during tracking phase

You can configure some of the parameters in the state diagram for the acquisition and tracking phase. You can set the SSA parameter (Group 4, APR 11) to allow for three, four, five, or six sync words before the decoder declares itself to be in synchronization. You can also set the SST parameter (Group 4, APR 11) to allow for two, three, four, or five misdetections sync words before the decoder declares a loss of synchronization. Figure 6.6 and Figure 6.7 show the minimum and maximum number of states that you can select for acquisition and tracking modes.

Figure 6.6
Minimum and Maximum
Number of States in the
Acquisition Phase

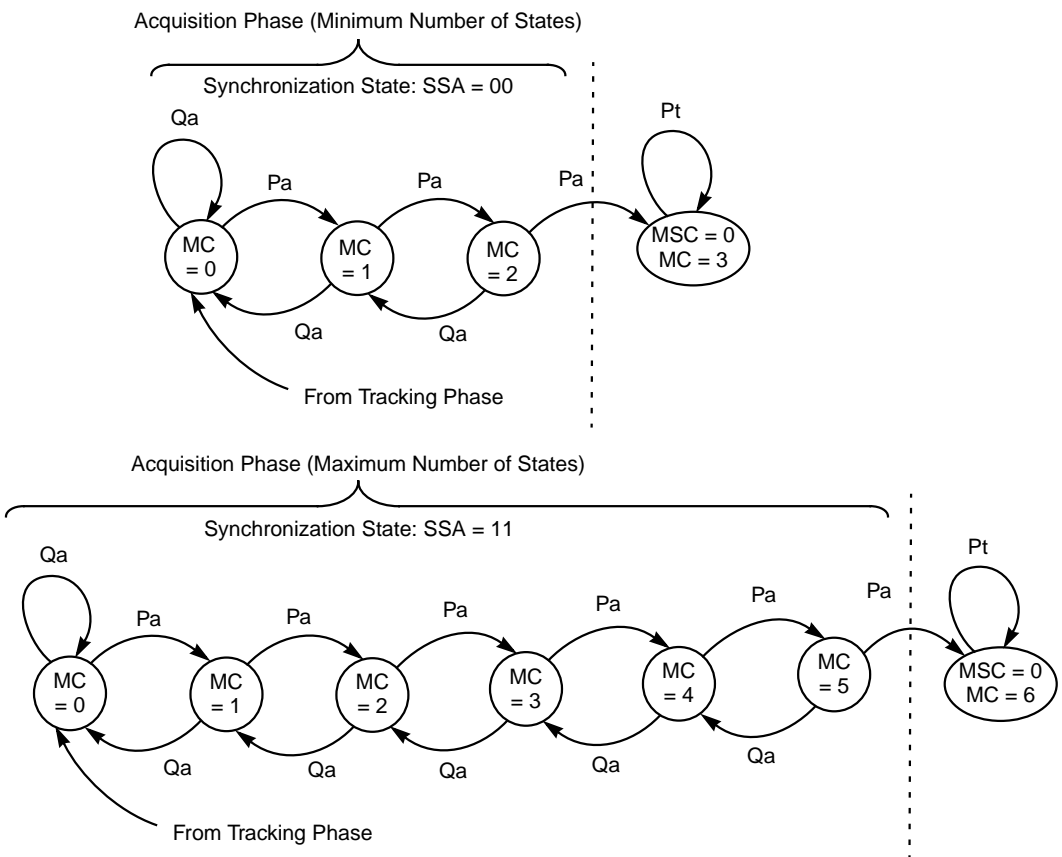
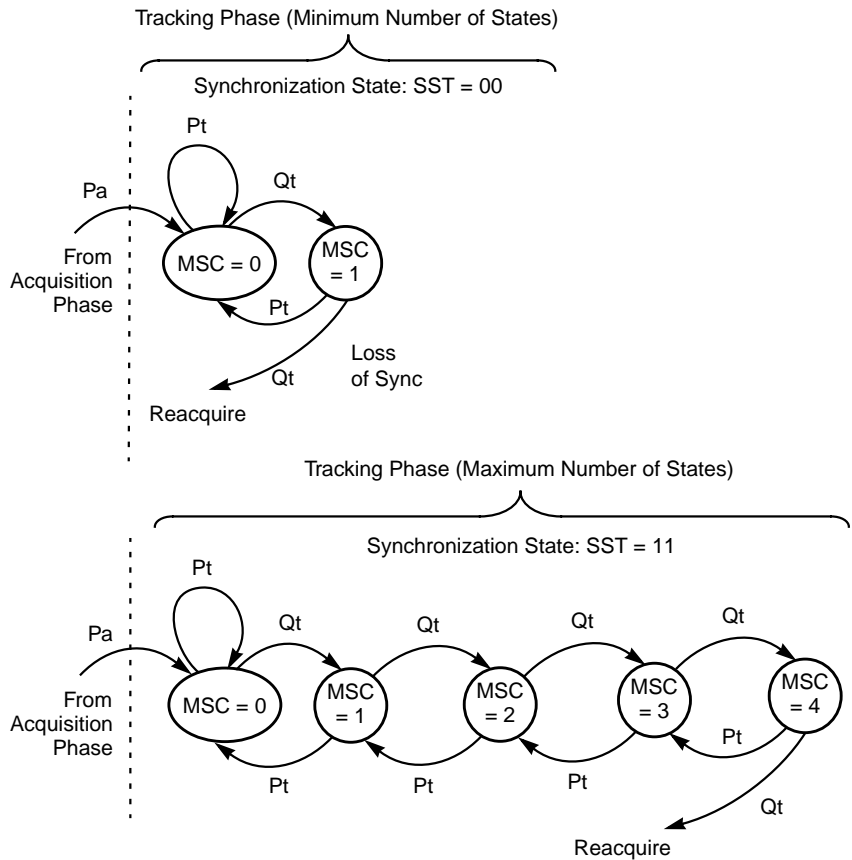


Figure 6.7
Minimum and
Maximum Number
of States in the
Tracking Phase



An MPEG-2 RS(204,188) protected transport packet consists of 204 bytes, including 1 sync byte, 187 data bytes, and 16 redundancy bytes. [Figure 6.8](#) shows the data format of the MPEG-2 Transport Packet.

Figure 6.8
MPEG-2 Transport
Packet

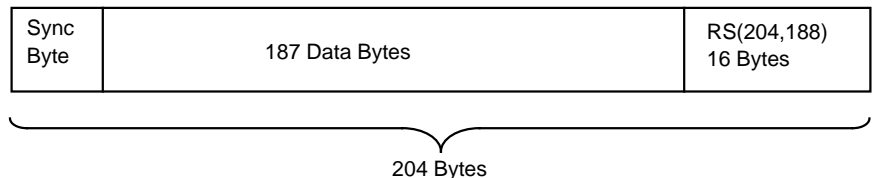


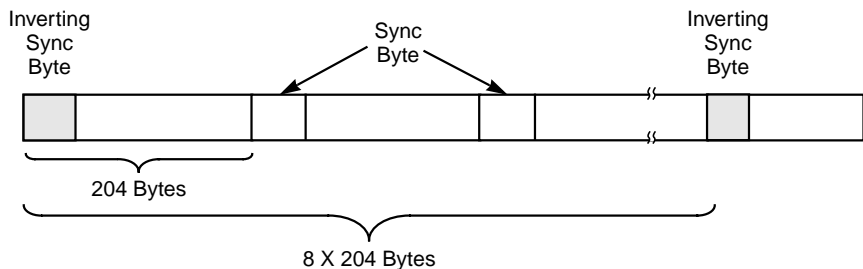
Table 6.1 shows the computed values for mean acquisition time (T_{ac}), mean time to loss of lock (T_{ll}), and probability of false lock (P_{fl}) for synchronization stage 2 as a function of the incoming bit error rate (code word length = 204 bytes, sync word length = 8 bits, $K = 0$, $L = 2$, 60 Mbits/s):

Table 6.1
Stage 2
Synchronization Values

Bit Error Rate	T_{ac}		T_{ll}		P_{fl}
	# frames	sec	# frames	sec	sec
5.0e - 04	3.88	1.05e - 04	9.00e + 15	2.44e + 11	5.98e - 08
1.0e - 03	3.91	1.06e - 04	9.00e + 15	2.44e + 11	5.98e - 08
2.0e - 03	3.98	1.07e - 04	9.00e + 15	2.44e + 11	5.98e - 08
5.0e - 03	4.16	1.12e - 04	4.50e + 15	1.22e + 11	5.98e - 08
1.0e - 02	4.48	1.21e - 04	6.37e + 12	1.72e + 08	5.98e - 08
2.0e - 02	5.15	1.39e - 04	1.39e + 10	3.78e + 05	5.98e - 08
5.0e - 02	7.23	1.98e - 04	5.21e + 06	1.41e + 02	5.98e - 08

For an expected BER of $1.0e - 03$, the decoder requires about four frame times to establish synchronization, and loss of sync occurs after $9.0e + 15$ frames. With one modification, the DVB Standard of the European Broadcast Union has adopted this basic format as a standard for multiprogram TV via satellite. One out of every eight synchronization words in the data stream is mod 2 complemented. Figure 6.9 shows the data format of the L64704 transport packet.

Figure 6.9
L64704 Transport Packet



Given a bit stream that consists of a sequence of these packets, the second synchronization stage searches for the predefined sync byte and, upon having met the synchronization acquisition criteria, issues the control strobes for the modules that follow.

In addition to providing the proper data alignment for the following Deinterleaver and Reed-Solomon Decoder modules, the second synchronization stage resolves the 180-degree phase uncertainty that the upstream demodulator may have introduced. The first (Viterbi) synchronization stage is not able to detect this source of error. During the acquisition phase, the decoder simultaneously looks for the synchronization word and its complemented version to resolve the uncertainty.

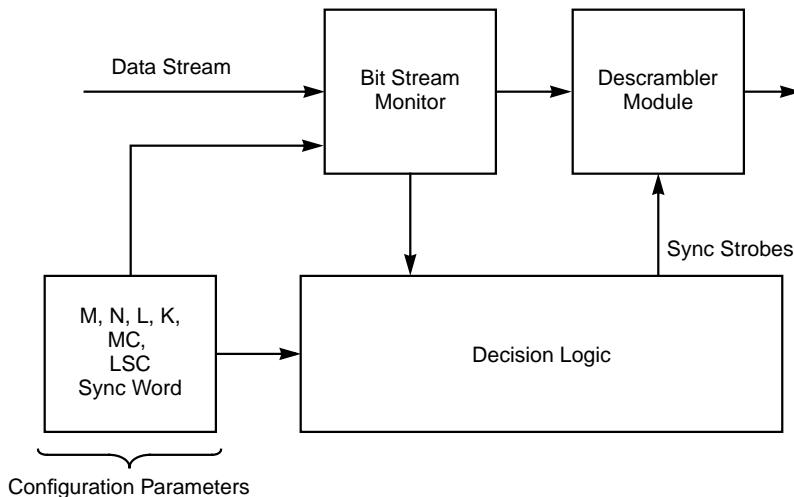
The decoder does not remove the sync byte from the data stream because it is part of the MPEG system layer syntax, and therefore the channel decoding operation leaves it undisturbed.

6.4
Descrambler
Synchronization

This section describes the third stage synchronization; Descrambler synchronization. Figure 6.10 illustrates the Descrambler synchronization process.

The L64704 restarts the Descrambler every 8 N byte times. The L64704 aligns this restart with the complemented synchronization word that is present in the data stream once every eight Reed-Solomon code words (once every 8 N bytes).

Figure 6.10
Descrambler
Synchronization

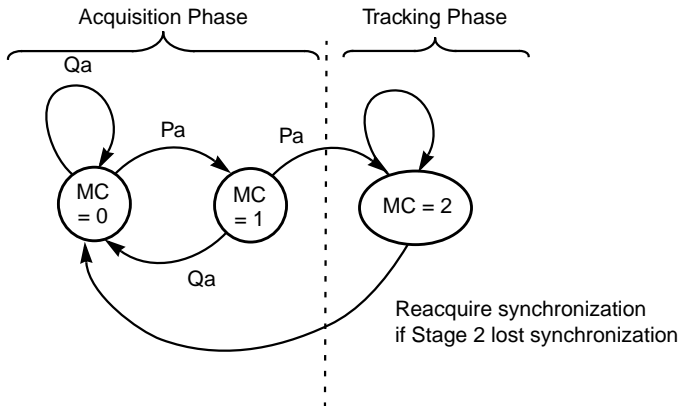


For this third stage synchronization, the L64704 uses an approach very similar to that used in the second synchronization stage during the acquisition phase to ensure proper data alignment. Because the detection of an out-of-synchronization condition in the second stage automatically

forces the third stage to reacquire, the tracking phase for the third synchronization stage is simpler. Figure 6.11 shows a state diagram that outlines how the decoder determines synchronization, tracking, and loss of synchronization for the third stage.

Note that in this stage, any noninverting corrupted sync bytes found in the tracking phase are duly replaced by the original predefined noninverting sync byte.

Figure 6.11
Synchronization,
Tracking, and Loss
of Synchronization
in the Descrambler



Pa: State Transition, Inverting Sync Word Detected (8N, M, K)
Qa: State Transition, Inverting Sync Word Misdetected

Chapter 7

The FEC Decoder Pipeline

This chapter discusses the DEC Decoder Pipeline. The decoder pipeline consists of four modules that are connected in a logical sequence. This chapter discusses the four modules in the pipeline in five sections:

- ◆ [Section 7.1, “Viterbi Decoder Module,”](#) provides details on the L64704's Viterbi Decoder module.
- ◆ [Section 7.2, “Deinterleaver Module,”](#) describes the Deinterleaver module.
- ◆ [Section 7.3, “Reed-Solomon Decoder,”](#) discusses the L64704's Reed-Solomon Decoder.
- ◆ [Section 7.4, “Descrambler Module Architecture and Operation,”](#) provides details on the Descrambler module.
- ◆ [Section 7.5, “FEC Module Software Reset”](#) describes the use of the FEC_Reset bit.

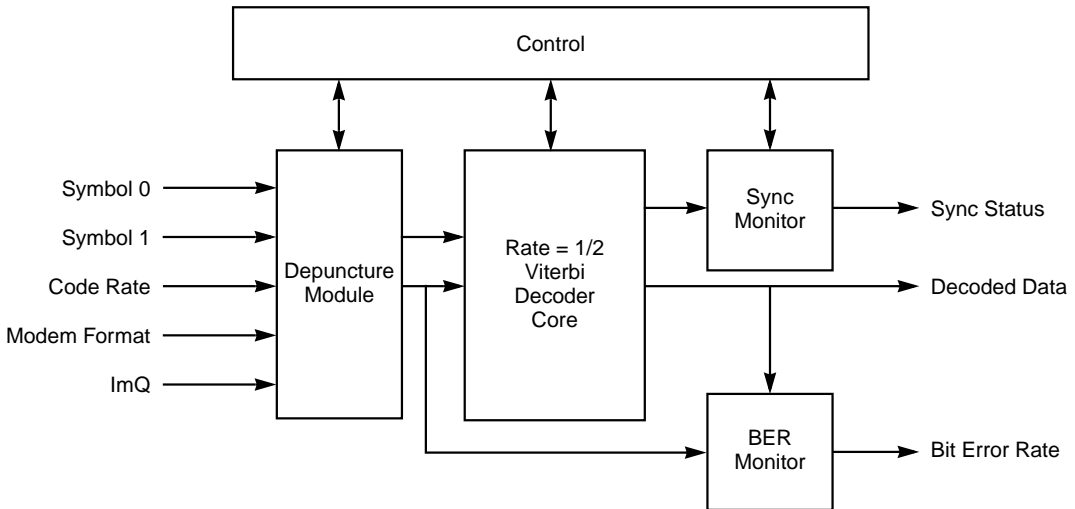
7.1 Viterbi Decoder Module

The Viterbi Decoder contains the following major modules:

- ◆ A depuncturing module for code rates other than 1/2
- ◆ A 1/2 code rate Viterbi decoder core that computes the serial output data stream given two sets of soft decision data input streams
- ◆ A synchronization monitoring block to provide information on acquisition or loss of synchronization
- ◆ A bit error rate monitoring block
- ◆ A control module

The block diagram in [Figure 7.1](#) shows the relation of each of these modules to the other.

Figure 7.1
Block Diagram of
Viterbi Decoder Core



7.1.1 Features

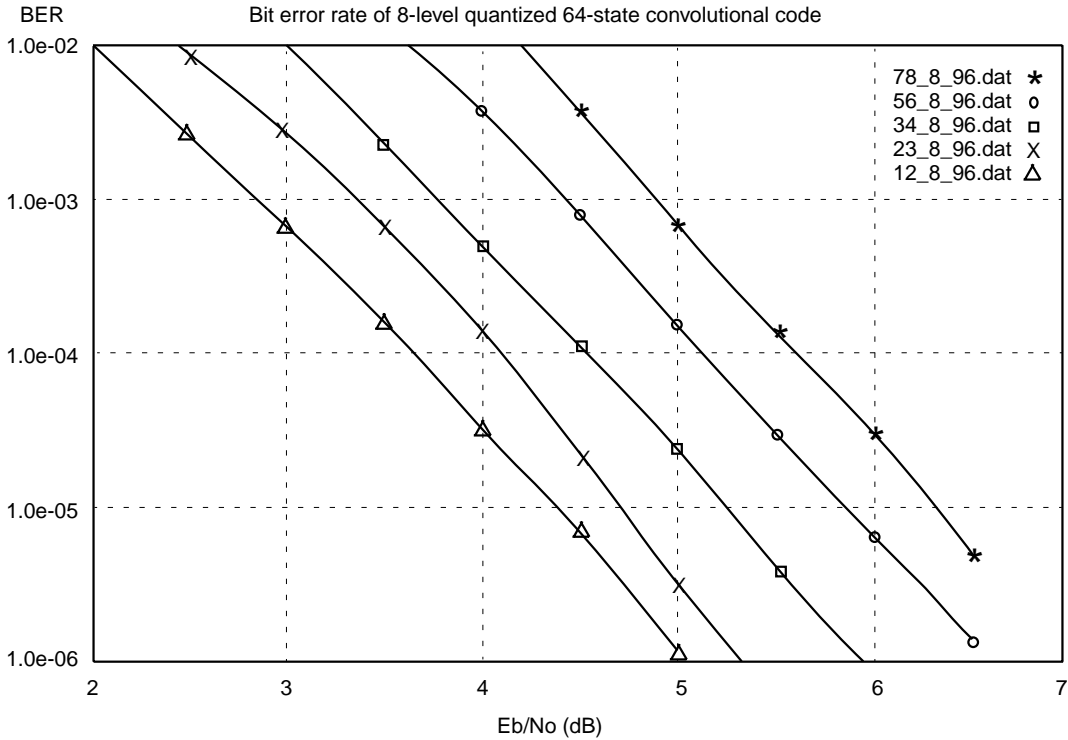
The Viterbi decoder module has the following features:

- ◆ A Viterbi Decoding Core with a basic rate equal to 1/2
- ◆ Compliant with European Digital Video Broadcast (DVB) Association (V4/MOD-B) standards
- ◆ Depuncturing for code rates equal to 1/2, 2/3, 3/4, 5/6, and 7/8
- ◆ Accepts input in binary offset or sign magnitude format
- ◆ Constraint length (K) of seven
- ◆ Synchronization monitor
- ◆ Decoded Bit Error Rate (BER) monitor
- ◆ Maximal Likelihood (ML) decoding algorithm
- ◆ 5.2 dB coding gain for rate equal to 1/2 (no erased input) code at BER of $1e - 5$
- ◆ Generating Polynomial 171 (Octal) and 133 (Octal)

**7.1.2
Code
Performance**

The code performance for the Viterbi decoder is based on a simulation of a numerically accurate model of the architecture. Figure 7.2 shows the results for a constraint length (K) of seven and code rates of 1/2, 3/4 and 7/8 that were seen on a small sampling of Satellite Decoder Evaluation boards. Your results may be different.

Figure 7.2
Code Performance for
Viterbi Decoder



**7.1.3
Punctured
Codes**

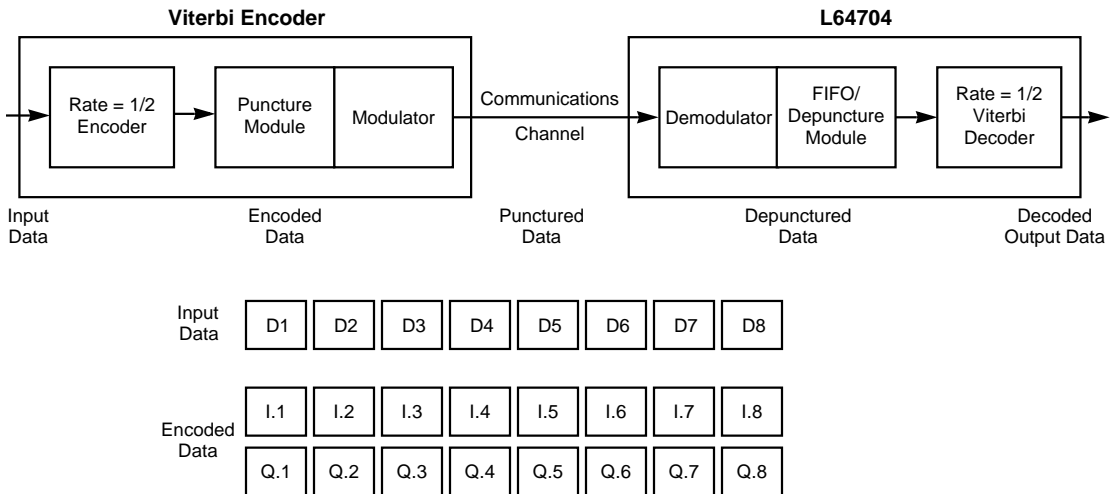
The L64704 supports not only the basic rate equal to 1/2 decoding operations, but also code rates equal to 2/3, 3/4, 5/6 and 7/8. The code rate and underlying depuncture scheme chosen dictates the proper sequence of symbols on the DEM_I and DEM_Q inputs. Table 7.1 shows the puncture patterns for various code rates.

Table 7.1
Puncture Patterns
for Various Code
Rates

Code Rate	Puncture Pattern
1/2	DEM_I: 1 DEM_Q: 1
2/3	DEM_I: 1 0 DEM_Q: 1 1
3/4	DEM_I: 1 0 1 DEM_Q: 1 1 0
5/6	DEM_I: 1 0 1 0 1 DEM_Q: 1 1 0 1 0
7/8	DEM_I: 1 0 0 0 1 0 1 DEM_Q: 1 1 1 1 0 1 0

Figure 7.3 shows a block diagram of the puncturing and depuncturing process for a rate 1/2 encoder. For each data bit D_n , the upstream encoder generates two corresponding encoded data symbols, $I.n$ and $Q.n$. By deleting or *puncturing* some of the encoded data symbols, the puncturing process allows a rate 1/2 encoder to generate codes of higher rates. The L64704's depuncturing module allows its rate 1/2 decoder to decode data transmitted at higher code rates. Figure 7.4 illustrates the puncture patterns for different code rates.

Figure 7.3
Puncturing and
Depuncturing Block
Diagram



The L64704 receives the encoded data symbols in QPSK or BPSK format on the RI[5:0] and RQ[5:0] buses. The L64704 receives these symbols in the order shown on the right of L64704 Input Data in [Figure 7.4](#). The depuncturing module handles the reordering and the insertion of erasures into the received symbol stream before the rate equal to 1/2 Viterbi decoder module starts decoding.

Figure 7.4
Puncture Pattern
for Different Code
Rates

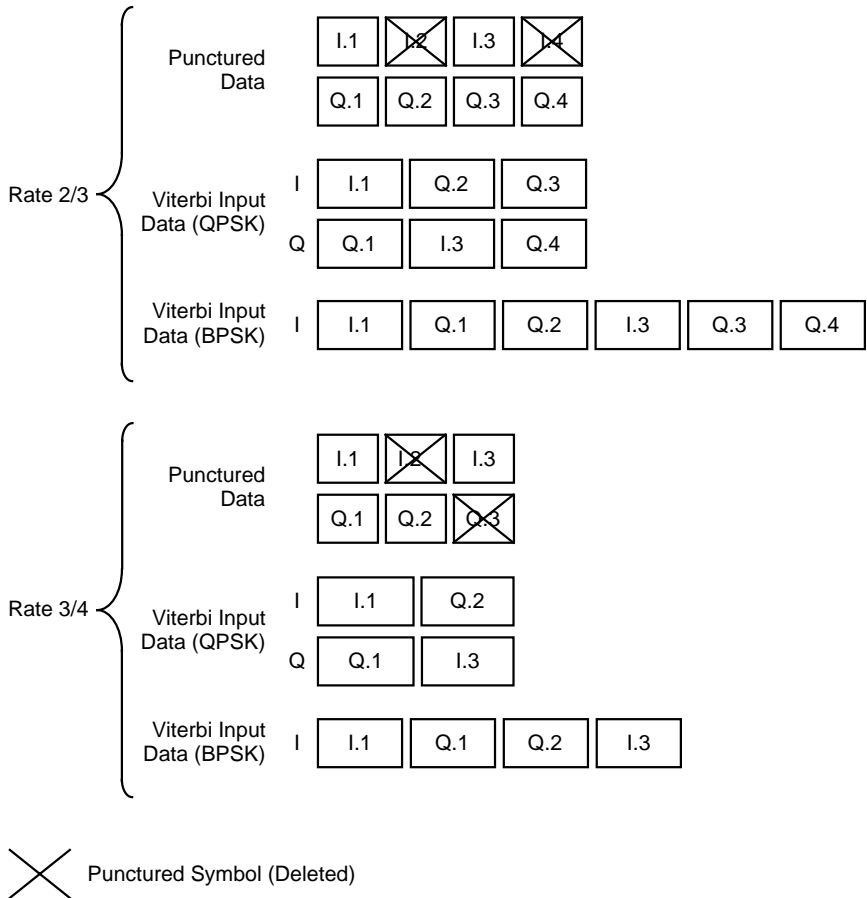
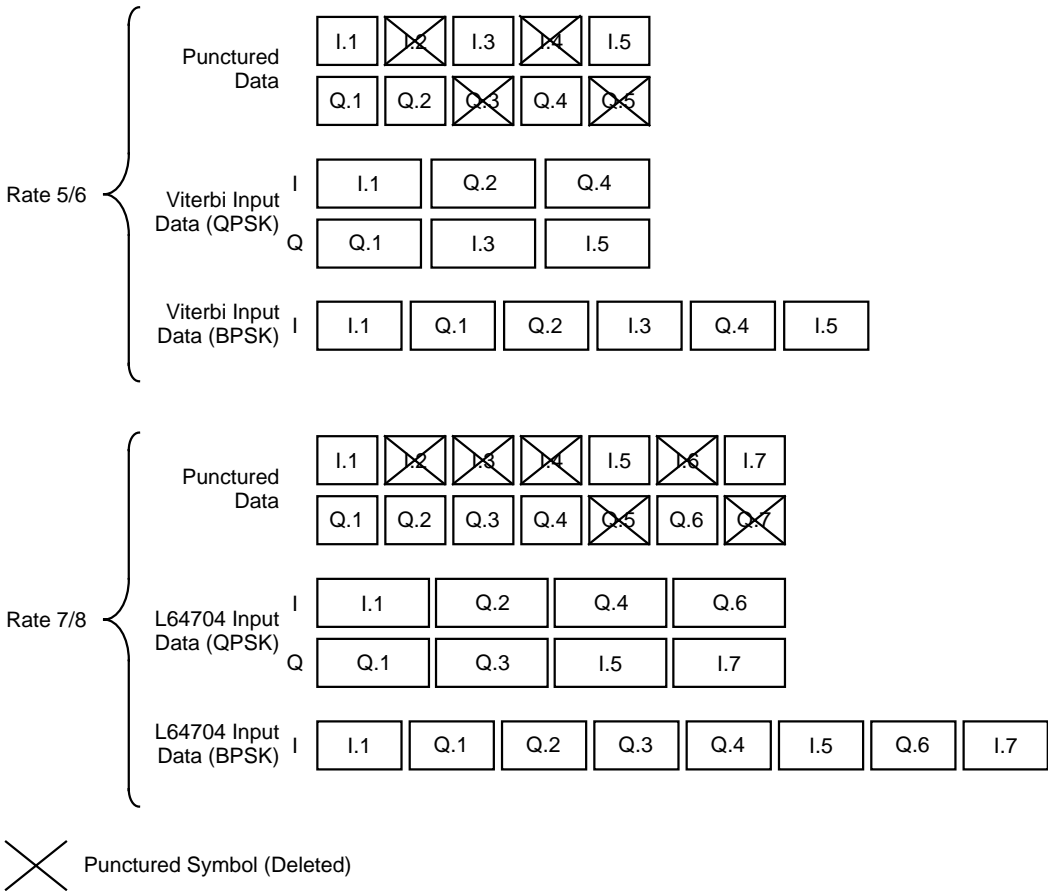


Figure 7.4 (Cont.)
Puncture Pattern for
Different Code Rates



7.1.4 Viterbi Bit Error Rate Monitor

A performance monitor for the channel bit error rate (BER) is built into the L64704. The monitor compares an appropriately delayed version of the incoming channel data stream to the re-encoded Viterbi decoder output data stream to find occurrences of bit errors. Figure 7.5 shows a block diagram of the Viterbi bit error detection circuit.

The Viterbi decoder core latency delays depunctured data. The rate equal to 1/2 Viterbi decoder core produces a decoded bitstream that is being convolutionally re-encoded. This results in a symbol stream that can be compared on a symbol-by-symbol basis against the incoming

depunctured channel stream. Any discrepancy between two respective symbols indicates a corrected error (or with a much smaller probability, an erroneous output bit produced by a failure of the Viterbi decoder to decode correctly). For code rates other than rate equal to 1/2, the decoder disregards input symbols marked as erasures when it detects the error events.

The decoder processes the bit error events further to produce a measure of the actual channel bit error rate. The register VMDC2 (Group 4, APR 5:7) specifies the number of channel bits (and therefore the time period), divided by four, over which the decoder counts the number of occurring channel bit errors. Refer to Group 4, APR 5:7 or [page 3-31](#) for a description of VMDC2.

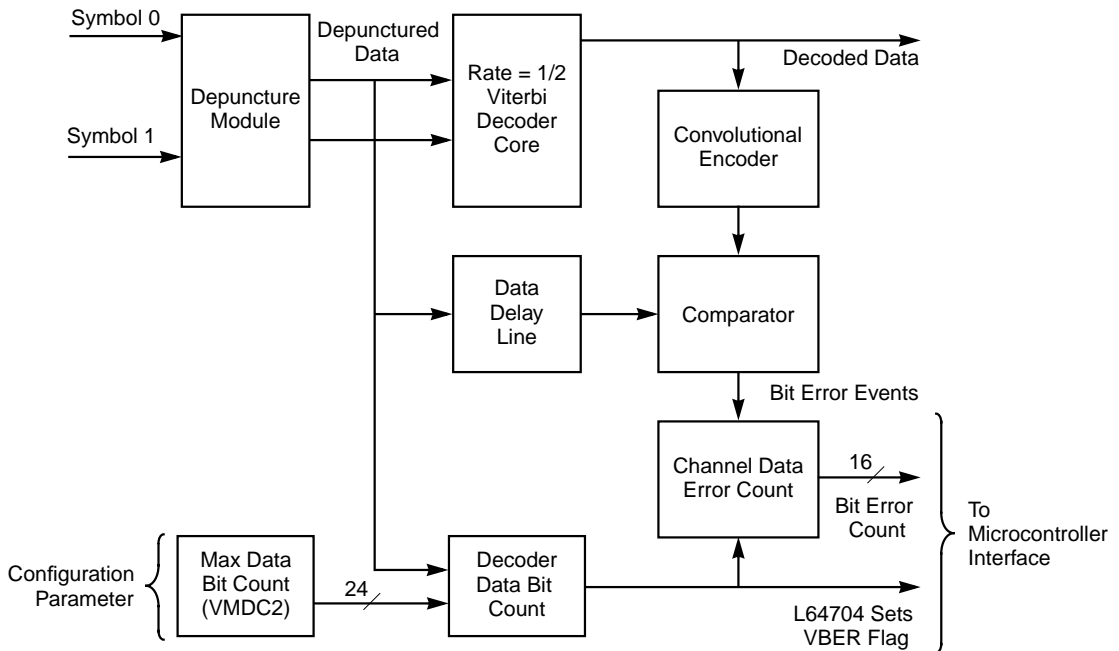
The channel data error counter accumulates the errors internally and updates the Viterbi Bit Error Rate Count (VBERC, Group 3, APR 4:5) once at the end of the period specified by VMDC2. You can read the value of the VBERC using the microcontroller interface. VBERC contains the number of errors divided by four. In addition, the L64704 sets the VBER flag in the System Status Register (Group 2). This flag indicates that the decoder has reached the period specified by VMDC2. The decoder asserts $\overline{\text{INT}}$ if the corresponding interrupt enable bit, VBER_IE, is set in the System Mode Register (Group 2). Refer to [Section 3.4, “Group 2 Registers”](#) on [page 3-11](#) for details.

Typical threshold values for each puncturing rate in the case of a standard DVB application are shown in [Table 7.2](#):

Table 7.2
Viterbi Threshold
Values

Puncturing Rate	1/2	2/3	3/4	5/6	7/8
VMDC1	0x40	0x40	0x40	0x40	0x40
VMBEC	0x1E	0x0E	0x0A	0x07	0x05
Ratio	23.6%	11.1%	8.0%	5.6%	4.1%

Figure 7.5
Block Diagram of
Viterbi Bit Error
Detection Circuit



To assist the proper selection of the ratio of the threshold values VMDC1 and VBERC, [Figure 7.6](#) through [Figure 7.10](#) show the plots of the percentages of symbol errors vs. E_b/N_0 for all the code rates that the L64704 supports. The upper curve in each graph represents the out-of-synchronization condition, and the lower curve represents the in-synchronization condition.

Figure 7.6
Percent Channel
Symbol Errors vs.
Eb/No for
Rate = 1/2 Code

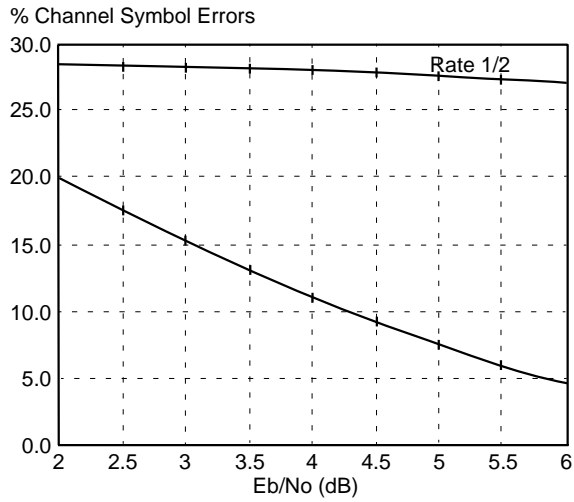


Figure 7.7
Percent Channel
Symbol Errors vs.
Eb/No for
Rate = 2/3 Code

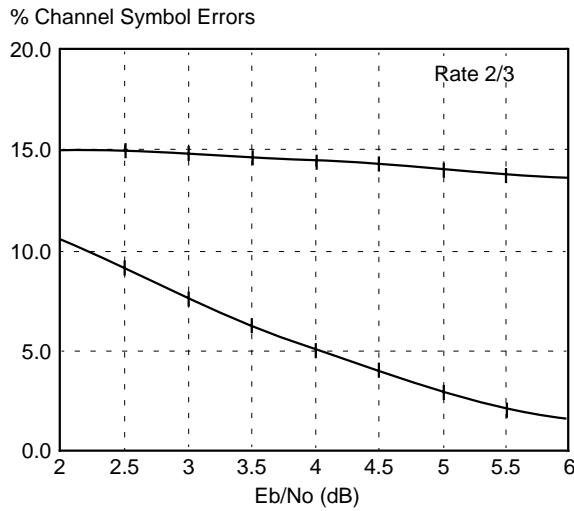


Figure 7.8
Percent Channel
Symbol Errors vs.
 E_b/N_0 for
Rate = 3/4 Code

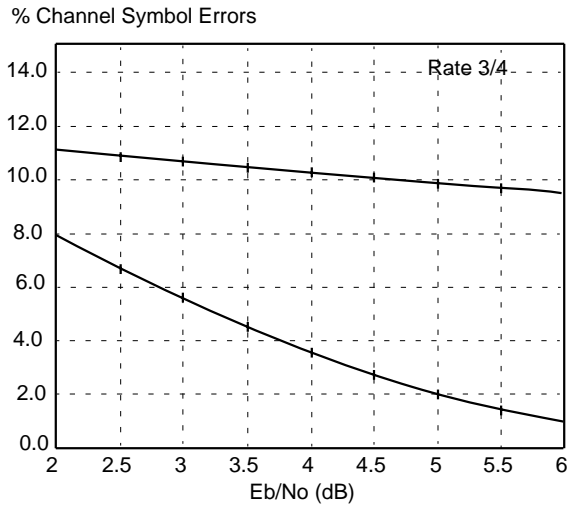


Figure 7.9
Percent Channel
Symbol Errors vs.
 E_b/N_0 for
Rate = 5/6 Code

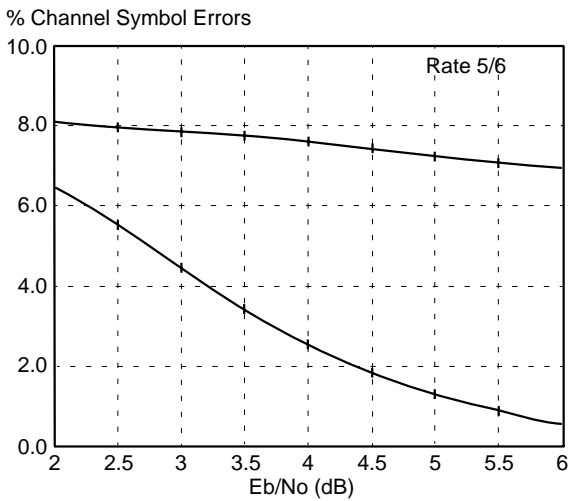
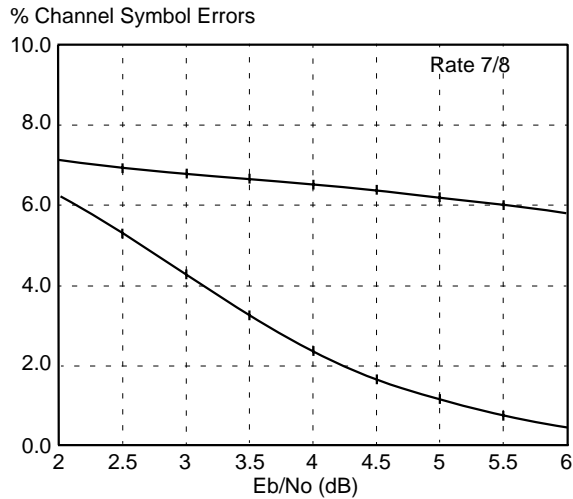


Figure 7.10
Percent Channel
Symbol Errors vs.
Eb/No for
Rate = 7/8 Code



You must select a value for the ratio $VMBEC/VMDC1$ that is in between the in-synchronization and the out-of-synchronization curves. For example, for a rate equal to 1/2 code, a value of 0.24, or 24%, for $VMBEC/VMDC1$ establishes a valid decision threshold over the entire E_b/N_0 range shown. Equation 7.1 shows the computation of Channel Symbol Error Percentages.

Equation 7.1

$$\text{Channel Symbol Error Rate} = \frac{128VMBEC + 32}{256VMDC1}$$

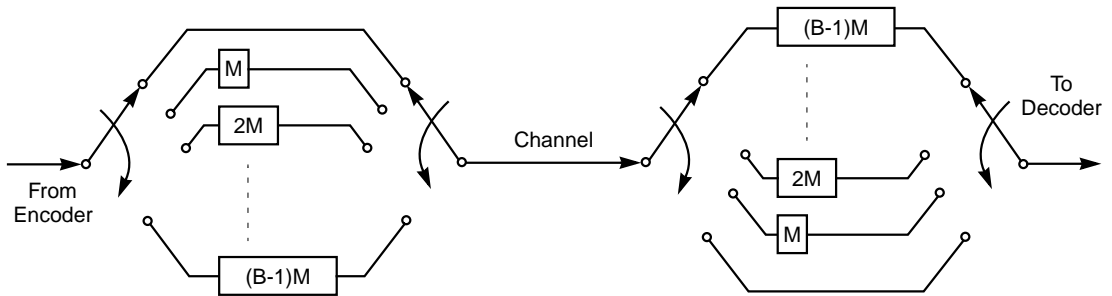
7.2 Deinterleaver Module

Figure 7.11 outlines the interleaving/deinterleaving operation. The Interleaver is a device that rearranges the ordering of a sequence of symbols in a deterministic manner. A (B, N) Periodic Interleaver has the following characteristics:

- ◆ The minimum separation at the Interleaver output is B symbols for any two symbols that are separated by less than N symbols at the Interleaver input.
- ◆ If the channel inserts any burst of less than B errors, single errors occur at the Deinterleaver output.

This scheme is also called a convolutional Interleaver/Deinterleaver.

Figure 7.11
Interleaving/
Deinterleaving
Operation



The L64704 Deinterleaver module performs periodic deinterleaving. The user must specify two parameters: B, the desired interleaving depth, and M, defined as:

$$M = \left\lceil \frac{N}{B} \right\rceil.$$

The L64704 Deinterleaver features:

- ◆ Convolutional deinterleaving
- ◆ Maximum block length of 204 bytes
- ◆ Deinterleaving depth of 12
- ◆ System clock rate up to 62.5 MHz

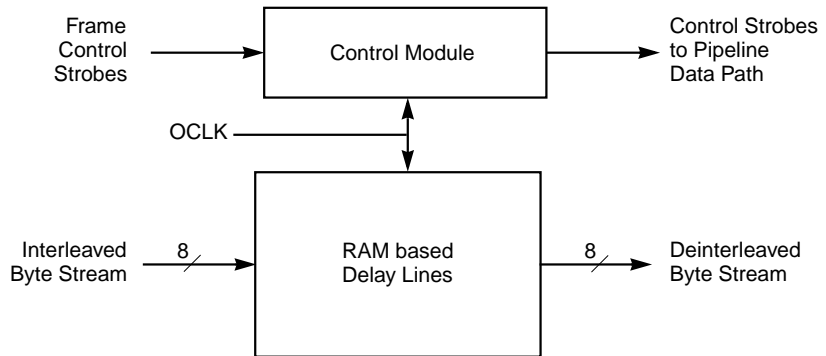
7.2.1 Deinterleaver Block Diagram

The Deinterleaver is comprised of two main modules:

- ◆ A set of configurable RAM-based delay lines that implement the proper delay for individual data bytes
- ◆ A controller that handles and generates the strobes needed by the following elements in the data path.

The modules are shown in the block diagram in [Figure 7.12](#).

Figure 7.12
Block Diagram of
Deinterleaver Core



7.2.2 Deinterleaver Output

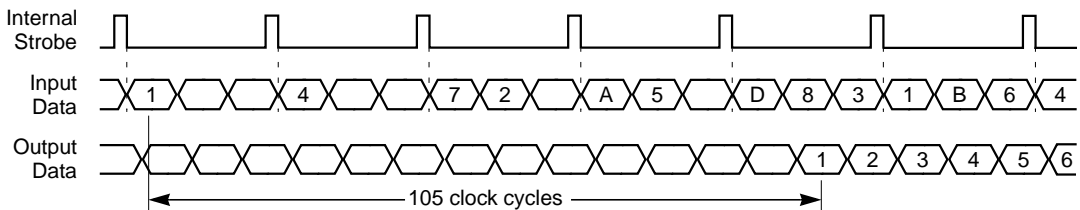
The Deinterleaver receives the rearranged byte stream and inverts the interleaver's function to reconstruct the original byte stream. The internal strobes indicate the block boundaries that the Deinterleaver must recover.

The Deinterleaver outputs the original byte stream after a delay given by:

Equation 7.2
$$Delay = \{(B - 1) \times B \times \lceil N/B \rceil + 1\} \times 8 + 1$$

Figure 7.13 shows an example in which the total delay is $\{2 \times 3 \times 2 + 1\} \times 8 + 1 = 105$ clock cycles. Notice that the delay from the first input byte to the first valid output byte is indeed 105 clock cycles.

Figure 7.13
Deinterleaver Output
Example



7.3 Reed-Solomon Decoder

The Reed Solomon Decoder is a Forward Error Correction unit that looks at the check bytes that are appended to the data stream and either corrects any errors that it finds in the data stream or asserts the ERROROUT pin when it cannot correct the data.

7.3.1 Terms and Concepts

Error Correction Code (ECC) devices have a specific lexicon associated with their ability to correct transmission messages. This section defines the terms used for variables in the Reed-Solomon Core. The terms are used throughout this document.

R **Check Bytes**
The encoder generates and appends check bytes to the incoming message according to the Reed-Solomon error correction encoding. The decoder uses check bytes to locate and correct errors caused by transmission. The system designer specifies the size of the check byte field within the limitations.

d **Detection power**
Detection power specifies the maximum number of detectable errors. Detection power has a minimum value of:

$$\left\lfloor \frac{R}{2} \right\rfloor \text{ and a maximum value of } R.$$

K **Message Length**
The message is comprised of multiple bytes. The size of the message varies, depending on the code word length and the check bytes used, where $K = N - R$.

m **Symbol Size**
A data transfer is comprised of multiple symbols and the symbol size, m , is eight bits.

N **Codeword Length**
This variable is the sum of the number of message bytes and the number of check bytes ($K + R$). The value of N is 204.

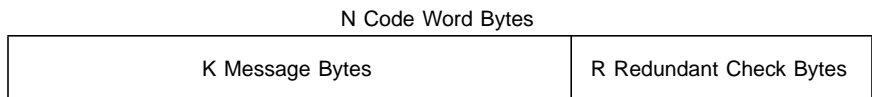
T **Number of Error Corrections**
This variable is the maximum number of error corrections performed by the decoder. The value of T is 8.

7.3.1.1 Forward Error Correction

Forward error correction requires an encoder that appends redundant check bytes to a message before transmission. The check bytes, with an indeterminate number of bits, are referred to as symbols. The message symbols followed by redundant check symbols are called code words. The check symbols are redundant in the sense that they are derived from the message and are appended to the message. Check symbols are also referred to as “redundant check bytes,” and sometimes as “correction bytes.”

Figure 7.14 illustrates a code word. Explanatory text follows the figure.

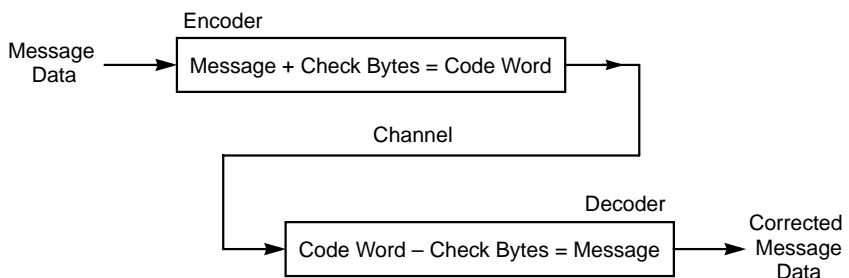
Figure 7.14
Code Word
Structure



A code word is a block of N bytes that includes K message symbols and $N - K$ check bytes (R). The check bytes or symbols are some fraction of the message symbols. A large number of check symbols allows the decoder to correct a large number of transmission errors.

The redundant check symbols in a message allow a decoder at the receiving end of a transmission line to detect transmission errors and reconstruct the original message content. Figure 7.15 shows a block diagram of the basic encoder and decoder functions in a transmission system.

Figure 7.15
Forward Error
Correction Data
Path



After generating a code word, the encoder transmits it through a low cost channel to a decoder. The decoder compares the bit stream in the message data to the encoding in the check bytes to detect transmission

errors. The original message can be precisely reconstructed from the check symbols, as long as the number of errors in the code word is less than or equal to $R/2$.

7.3.1.2 Reed-Solomon Correction Codes

Reed-Solomon (RS) error correction codes are systematic and operate on bytes rather than single-bit data streams. They are especially good in burst error applications. The importance of RS codes is illustrated by their adoption as international and domestic standards in various areas of applications. The codes are expressed by convention as two numbers, the first indicating the total codeword length (N), and the second indicating the number of message bytes (K). The difference between these two numbers (N – K) is the number of check bytes. A (255, 233) RS code, for instance, with eight-bit bytes, was adopted as part of the standard for space missions by both the European Space Agency and NASA. The compact disc digital-audio system uses a combination of a (32, 28) RS code and a (28, 24) RS code. The MIL-STD-2179/ANSI X3B.6 media exchange standard uses a (161, 153) RS code and a (128, 118) RS code for high-density magnetic recording.

The L64704 uses the following generator polynomial for RS codes:

$$\prod_{i=0}^{R-1} (x + \alpha^i)$$

where α is a root of the binary primitive polynomial:

$$x^8 + x^4 + x^3 + x^2 + 1$$

A data byte ($d_7, d_6, \dots, d_1, d_0$) is identified with the element $d_7a^7 + d_6a^6 + \dots + d_1a + d_0$ in $GF(256)$, the finite field with 256 elements.

The error correcting power of an RS code is related to the number of redundant check symbols in its code words. In general, an RS code with $2T$ check symbols per code word can correct up to T byte errors per code word. Higher redundancy allows more errors to be corrected

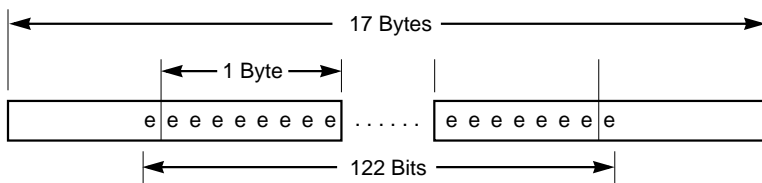
The remainder of this section describes the process of correcting transmission errors with Reed-Solomon codes.

7.3.1.3 Error Handling and Correction

A bit error occurs when a transmitted zero is received as a one or vice versa. A byte error occurs when one or more bits in the byte have errors. For example, a byte with only one bit error is counted as one byte error, and a byte with m bit errors (all bits are inverted) is also counted as one byte error. As long as a code word has no more than $T = \lfloor (R)/2 \rfloor$ byte errors, the RS Decoder corrects all errors. When a code word has more than $T = \lfloor (R)/2 \rfloor$ byte errors, the RS decoder detects the presence of excessive errors and asserts the $\overline{\text{ERROROUT}}$ signal to notify the user.

Assume that the byte size is 8, the redundant check parameter is 32, and a 122-bit burst error is input to the RS decoder. The RS decoder can correct up to $T = 16$ byte errors. A 122-bit burst can be divided into 17 bytes as shown in Figure 7.16, where each e represents a one bit error. Because the redundancy is 32, the decoder corrects up to 16 byte errors. Because the 122-bit burst corrupts 17 consecutive bytes, the maximum guaranteed correctable burst length in this example is 121 bits.

Figure 7.16
122-bit Burst
Example



7.3.2 Features

The Reed-Solomon Decoder features:

- ◆ 62.5 Mbits/s throughput
- ◆ Flag for corrected errors
- ◆ Complies with CCITT recommended CCIR723 standard for digital TV transmission
- ◆ DVB compliant
- ◆ Decoder channel output counts for uncorrected data and error vector data
- ◆ $\overline{\text{ERROROUT}}$ signal flags uncorrectable errors
- ◆ (204, 188) Reed-Solomon Code Format

7.3.3 Performance Analysis

The performance of the code against independent random byte errors can be computed by the equation:

Equation 7.3

$$q = \sum_{i=T+1}^N \frac{i}{N} \binom{N}{i} p^i (1-p)^{N-i}$$

where:

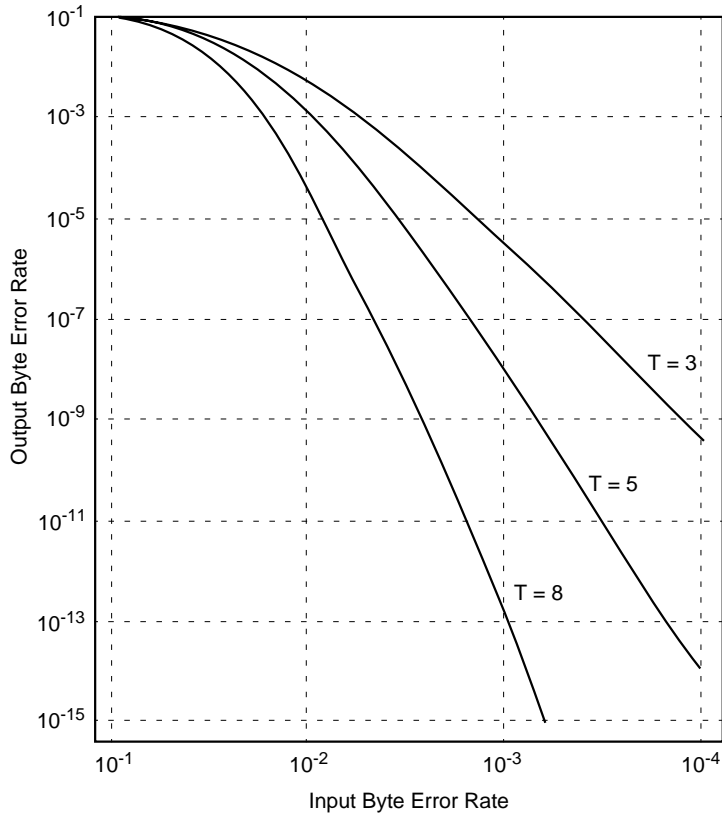
- N Code word length in bytes
- p Input byte error rate
- T Number of errors to correct
- q Output byte error rate
- $\binom{N}{i}$ Binomial coefficient that represents the number of ways of choosing i items from a collection of N distinct items

When more than T byte errors occur in a code word, the RS Decoders usually detect the presence of excessive errors and raise the uncorrectable error flag to notify the user. However, there is a small probability that the erroneous decoded code word remains undetected. The undetected erroneous code word rate is:

$$\frac{1}{T!} \left(\frac{N}{2^m - 1} \right)^T \sum_{i=T+1}^N \binom{N}{i} p^i (1-p)^{N-i}$$

For the code format (255, 223), the percentage redundancy of the RS code is $32/255 = 12.5\%$. With this modest amount of overhead, the coding system corrects error bursts of 16 bytes for $T = 16$. [Figure 7.17](#) illustrates the random error correction capability with a codeword length of 255 when various correction values expressed as T are programmed into the device.

Figure 7.17
(255, 255-2T)
Code Performance



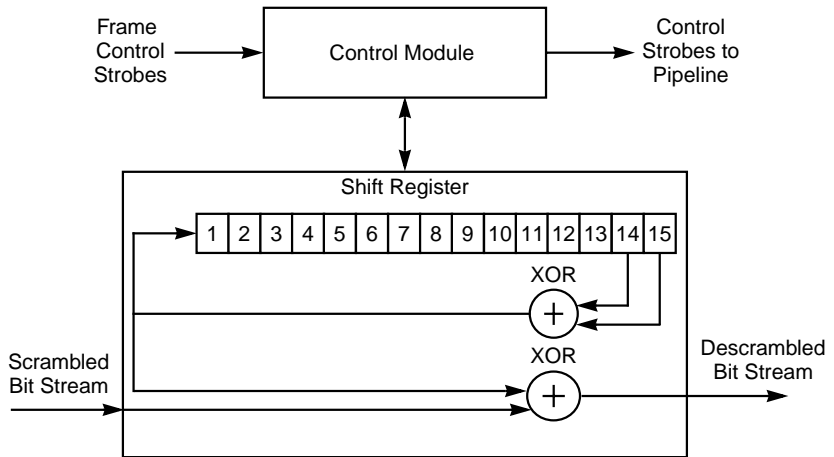
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7.4 Descrambler Module Architecture and Operation

Figure 7.18 shows a block diagram of the Descrambler. The Descrambler is composed of two modules:

- ◆ A module that generates a pseudorandom binary sequence (PRBS) that modifies the incoming data stream
- ◆ A control module that properly aligns data with the PRBS

Figure 7.18
Descrambler Block
Diagram

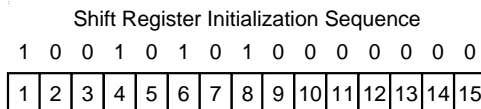


The following generator polynomial produces the pseudorandom bit sequence in the Descrambler:

$$1 + x^{14} + x^{15}$$

For initialization, a specific value is chosen for the 15-tap shift register shown in [Figure 7.19](#).

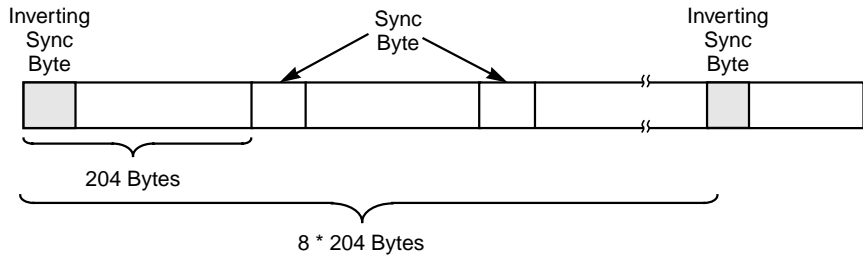
Figure 7.19
15-bit Shift
Register



The encoder inverts every eighth MPEG transport sync word (0x47) to generate a sync word (0xB8) that the decoder then uses to align the Descrambler with the incoming data stream. The first bit of the PRBS is applied to the first data bit following the inverting MPEG sync byte.

During the following seven noninverting MPEG sync words, the L64704 operates the Descrambler sequence generator, but does not modify the data stream. The L64704 resets the Descrambler after every inverting MPEG sync word.

Figure 7.20
Inverting Sync
Words in
Descrambler



7.5 FEC Module Software Reset

The L64704 resets the internal datapath and control modules for the FEC portion of the device when you set the FEC_Reset bit (Group 4, APR 36) to 1. The demodulator module is not affected. You do not need to set the bit back to 0 to complete the reset. The L64704 issues a single reset pulse each time the microcontroller writes a one to this bit. When the FEC_Reset bit is set, the L64704 resets the FEC processing unit and state machines to their initial states. The following operations occur when FEC_Reset is asserted:

- ◆ Internal datapath and control modules reset
- ◆ Group 4 registers unaffected by RESET
- ◆ Group 3 UEC and CEC counters reset
- ◆ DVALIDOUT pin set LOW
- ◆ FSTARTOUT pin set LOW
- ◆ $\overline{\text{ERROROUT}}$ pin set HIGH

Chapter 8

L64704 Specifications

This chapter provides the specifications for the L64704 Satellite Decoder from LSI Logic. The L64704 is implemented in LSI Logic's 0.5-micron, 3.3-volt LCB500K process.

This chapter contains the following sections:

- ◆ [Section 8.1, "Electrical Requirements,"](#) provides tables that describe the electrical characteristics of the L64704.
- ◆ [Section 8.2, "AC Timing,"](#) includes timing diagrams and tables that list the various AC timing parameters.
- ◆ [Section 8.3, "L64704 Packaging,"](#) shows the pinouts of the device, and provides the mechanical specifications for the package.

8.1 Electrical Requirements

This section specifies the electrical requirements for the L64704 device. Four tables list electrical data in the following categories:

- ◆ Absolute Maximum Ratings ([Table 8.1](#))
- ◆ Recommended Operating Conditions ([Table 8.2](#))
- ◆ Capacitance ([Table 8.3](#))
- ◆ DC Characteristics ([Table 8.4](#))
- ◆ Pin Description Summary ([Table 8.5](#))

Table 8.1
L64704 Absolute
Maximum Rating
(Referenced to
 V_{SS})

Symbol	Parameter	Limits ¹	Unit
V_{DD}	DC Supply Voltage	-0.3 to +3.9	V
V_{IN}	LVTTTL Input Voltage	-1.0 to $V_{DD} + 0.3$	V
V_{IN}	5 V Compatible Input Voltage	-1.0 to 6.5	V
I_{IN}	DC Input Current	± 10	mA
T_{STG}	Storage Temperature Range (Plastic)	-40 to +125	$^{\circ}\text{C}$

- Note that the ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation.

Table 8.2
L64704
Recommended
Operating
Conditions

Symbol	Parameter	Limits ¹	Unit
V_{DD}	DC Supply Voltage	+3.14 to 3.47	V
T_A	Operating Ambient Temperature Range (Commercial)	0 to +70	$^{\circ}\text{C}$
T_C	Case Temperature	0 to +85	$^{\circ}\text{C}$

- For normal device operation, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, may result in permanent device damage or impaired device reliability. Device functionality to stated DC and AC limits is not guaranteed if conditions exceed recommended operating conditions.

Table 8.3
L64704
Capacitance

Symbol	Parameter ¹	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

- Measurement conditions are $V_{IN} = 3.3$ V, $T_A = 25$ $^{\circ}\text{C}$, and clock frequency = 1 MHz.

Table 8.4 lists the DC characteristics of the L64704.

Table 8.4
L64704 DC
Characteristics

Symbol	Parameter ¹	Condition ²	Min	Typ	Max	Unit
V _{DD}	Supply Voltage		3.14	3.3	3.47	V
V _{IL}	Input Voltage LOW		V _{SS} - 0.5		0.2 V _{DD}	V
V _{IH}	Input Voltage HIGH	LVTTTL Com/Ind/Mil Temp Range	0.7 V _{DD}		V _{DD} + 0.3	V
		5-volt Compatible	0.7 V _{DD}		5.5	V
V _T	Switching Threshold			1.4	2.0	V
I _{IL}	Input Current Leakage	V _{DD} = Max, V _{IN} = V _{DD} or V _{SS}	-10	±1	10	mA
I _{IPU}	Input Current Leakage with Pull-up	V _{IN} = V _{SS}	-62	-215	-384	mA
I _{IPD}	Input Current Leakage with Pull-down	V _{IN} = V _{DD}	62	215	384	mA
V _{OH}	Output Voltage HIGH	I _{OH} = -1.0, -2.0, -4.0, -6.0, -8.0, -12.0 mA	2.4		V _{DD}	V
V _{OL}	Output Voltage LOW	I _{OH} = 1.0, 2.0, 4.0, 6.0, 8.0, 12.0 mA		0.2	0.4	V
I _{OZ}	3-state Output Leakage Current	V _{DD} = Max, V _{OUT} = V _{SS} or 3.5 V	-10	±1	10	µA
I _{OSP4}	Current P-Channel Output Short Circuit (4-mA Output Buffers) ³	V _{OUT} = V _{SS}	24		114	mA
I _{OSN4}	Current N-Channel Output Short Circuit (4-mA Output Buffers) ³	V _{OUT} = V _{DD}	-31	-60	-93	mA
I _{DD}	Quiescent Supply Current	V _{IN} = V _{DD} or V _{SS}			2	mA
I _{CC}	Dynamic Supply Current	f = 62.5 MHz, V _{DD} = Max		200		mA

1. To identify an input with an internal pull-up or pull-down resistor or an output's drive strength, see [Table 8.5, L64704 Pin Description Summary](#).
2. Specified at V_{DD} = 3.3 V ± 5% at ambient temperature over the specified range.
3. Not more than one output may be shorted at a time for a maximum duration of one second. The values specified are for the 4-mA output buffers. The values for other output buffers scale accordingly.

Table 8.5
L64704 Pin Description
Summary

Mnemonic	Description	Type	Drive (mA)	Active
A[2:0]	Address	TTL Input with Pull-down	–	–
\overline{AS}	Address strobe	TTL Input with Pull-up	–	LOW
BCLKOUT	Byte Clock Out	Output	4	–
CAR_DCLKP	Pre-scaled Carrier VCO	PECL/CMOS/TTL Input	–	DIFF
CAR_DCLKN	Pre-scaled Carrier VCO	PECL/CMOS/TTL Input	–	DIFF
CAR_PED[1:0]	Phase Error Detector to DAC	Output	4	–
CAR_VCO1P	Carrier Loop Control	Differential 3-state Output	4	–
CAR_VCO1N	Carrier Loop Control	Differential 3-state Output	4	–
CAR_VCO2P	Carrier Loop Control	Differential 3-state Output	4	–
CAR_VCO2N	Carrier Loop Control	Differential 3-state Output	4	–
CLK	R/Q Samples Clock	TTL Input	–	–
CLK_VCO_P	Clock Loop Control	Differential 3-state Output	4	–
CLK_VCO_N	Clock Loop Control	Differential 3-state Output	4	–
CO[7:0]	Channel Output	3-State Output	4	–
\overline{COE}	Channel Output Enable	TTL Input with Pull-up	–	LOW
\overline{CS}	Chip Select	TTL Input with Pull-up	–	LOW
D[7:1]	Data	Bidirectional TTL	4	–
D[0]	Data	Bidirectional TTL	4	–
\overline{DTACK}	Data Acknowledge	3-State Output	4	LOW
DVALIDOUT	Data Valid Output	Output	4	HIGH
$\overline{ERROROUT}$	Uncorrected Error Flag	3-State Output	4	LOW
FSTARTOUT	Framestart Output	Output	4	HIGH
HOST_MODE	Interface Selector	Input	–	HIGH
IDDTN	Test Pin	Input	–	HIGH
\overline{INT}	Interrupt	3-State Output	4	LOW
LP2	PLL Loop Filter	Input	–	–
OCLK	FEC Clock	Input	–	–
PCLK	PLL Output Clock	Output	4	–
PLLVDD	PLL V _{DD}	Input	–	–
PLLVSS	PLL V _{SS}	Input	–	–
PLLAGND	PLL Analog Ground	Input	–	–

(Sheet 1 of 2)

Table 8.5 (Cont.)
L64704 Pin Description
Summary

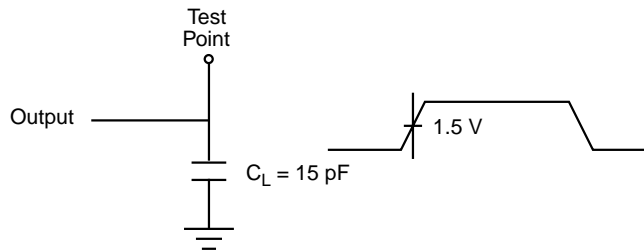
Mnemonic	Description	Type	Drive (mA)	Active
PWRP	Power Loop Control	3-State Output	6	HIGH
READ	Read Write	TTL Input with Pull-up	–	HIGH
RESET	Chip Reset	TTL Input	–	HIGH
RI[5:0]	Received I Samples	TTL Inputs	–	–
RQ[5:0]	Received Q Samples	TTL Inputs	–	–
SDATA	Serial Interface Data	Bidirect	4	–
SYNC/SCLK	Sync Status Flag	Output	4	–
XCTR_OUT[3:0]	External Controls	CMOS Outputs	4	–
XCTR_IN	External Controls	CMOS Input	–	–
XOIN	Input from External Crystal	CMOS Input	–	–
XOOUT	Output to External Crystal	CMOS Output	40	–

(Sheet 2 of 2)

8.2 AC Timing

This section presents AC timing information for the L64704. During AC testing, HIGH inputs are driven to 3.0 V and LOW inputs are driven at 0 V. For transitions between HIGH, LOW, and invalid states, timing measurements are made at 1.5 V, as shown in [Figure 8.1](#).

Figure 8.1
AC Test Load and
Waveform for
Standard Outputs



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For 3-state outputs, timing measurements are made from the point at which the output turns ON or OFF. An output is ON when its voltage is greater than 2.5 V or less than 0.5 V. An output is OFF when its voltage is less than $V_{DD} - 0.5 \text{ V}$ or greater than 0.5 V, as shown in [Figure 8.2](#).

Figures [8.3](#) through [8.7](#) show the various timing diagrams for the L64704. The numbers shown in the diagrams refer to parameters shown in [Table 8.6](#).

Figure 8.2
AC Test Load and
Waveform for
3-State Outputs

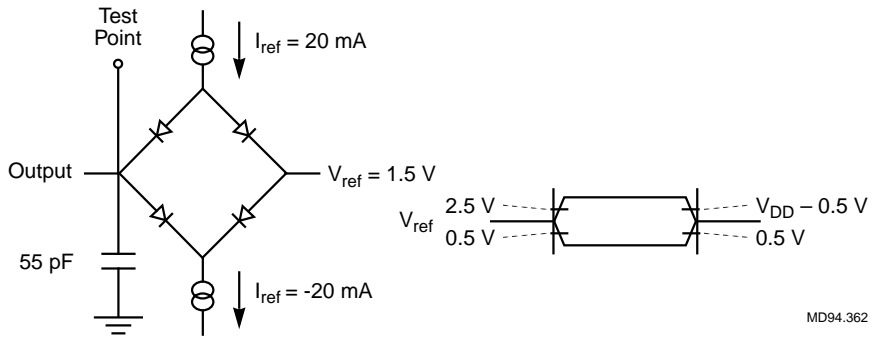


Figure 8.3
L64704
Synchronous AC
Timing

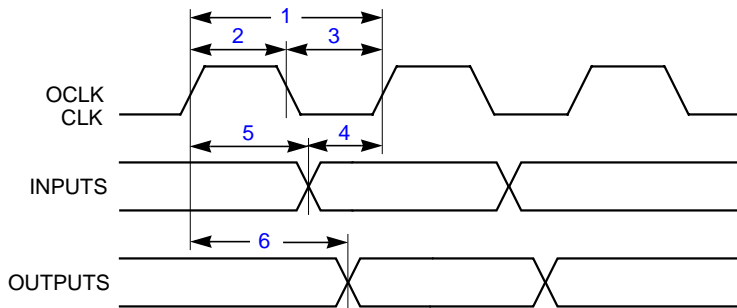


Figure 8.4
L64704 RESET
Timing Diagram

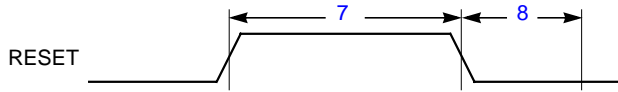


Figure 8.5
L64704 Bus
3-State Delay
Timing

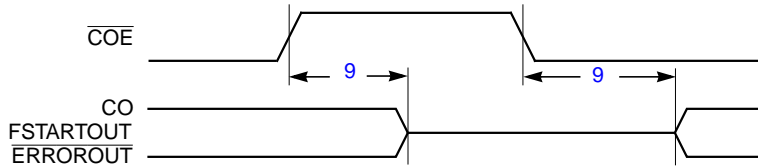


Figure 8.6
L64704 Decoder
Read Cycle

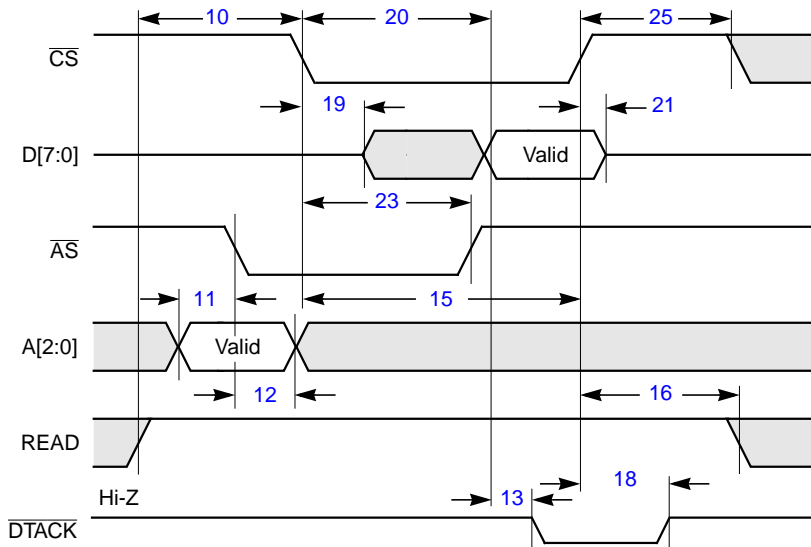
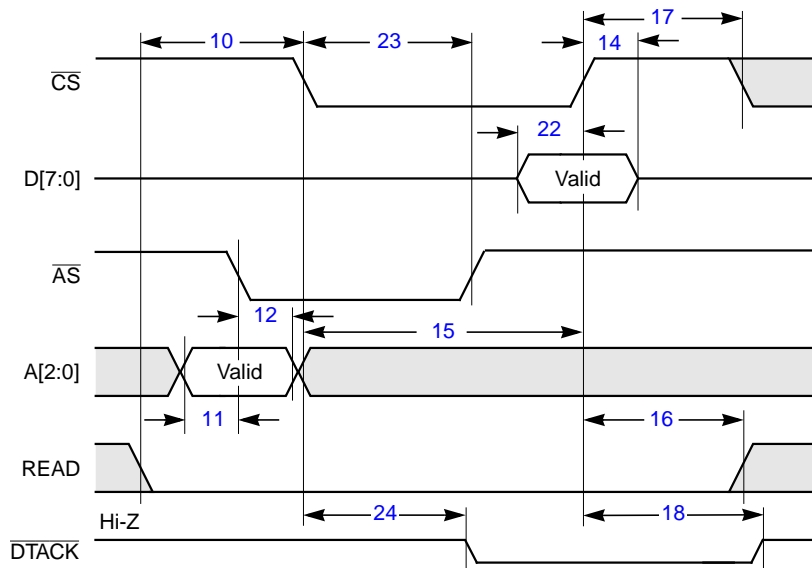


Figure 8.7
L64704 Decoder
Write Cycle



The numbers in column 1 of [Table 8.6](#) refer to the timing parameters shown in the preceding figures. All parameters in the timing tables apply for $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$ and a capacitive load of 15 pF.

Table 8.6
L64704 AC Timing
Parameters

Parameter	Description	Groups ¹	62.5 MHz		Unit
			Min	Max	
1	t_{CYCLE}	Clock Cycle OCLK, CLK	16.0	–	ns
2	t_{PWH}	Clock Pulse Width High	7.0	–	ns
3	t_{PWL}	Clock Pulse Width Low	7.0	–	ns
4	t_{S}	Input Setup Time to CLK	3.0	–	ns
5	t_{H}	Input Hold to CLK	1.0	–	ns
6	t_{OD}	Output Delay from OCLK	3.0	12.0	ns
7	t_{RWH}	Reset Pulse Width High	3	–	OCLK Cycles
8	t_{WK}	Wake-up Time	280	–	OCLK Cycles
9	T_{DLY}	Delay from $\overline{\text{COE}}$	–	15.0	ns

(Sheet 1 of 2)

Table 8.6 (Cont.)
L64704 AC Timing
Parameters

Parameter	Description	Groups ¹	62.5 MHz		Unit
			Min	Max	
10	t_{SURCS}	READ Setup Before \overline{CS} Low	0.0	–	ns
11	t_{SUA}	A[2:0] Setup Before \overline{AS} Low	15.0	–	ns
12	t_{HLDA}	A[2:0] Hold After \overline{AS} Low	Groups 0,1,4 Groups 2,3	0.0 3.0	– ns OCLK Cycles
13	t_{DCSDTL}	Data Valid to \overline{DTACK} Low	Groups 0,1,4 Groups 2,3	– 25.0 3.0	ns OCLK Cycles
14	t_{HLDD}	Write Data Hold After \overline{CS} High		0.0	– ns
15	t_{CYCLE_CS}	Minimum \overline{CS} Width	Groups 0,1,4 Groups 2,3	30.0 4.0	– ns OCLK Cycles
16	t_{HLDRCS}	READ Hold After \overline{CS} High		0.0	– ns
17	t_{WRREC}	Write Recovery Time	Groups 0,1,4 Groups 2,3	30.0 3.0	– ns OCLK Cycles
18	t_{DCSDTH}	\overline{CS} High to \overline{DTACK} High	Groups 0,1,4 Groups 2,3	– 40.0 5.0	ns OCLK Cycles
19	t_{DELZL}	\overline{CS} Low to Data Driven	Groups 0,1,4	9.0	– ns
20	t_{DELD}	\overline{CS} Low to Data Valid	Groups 0,1,4 Groups 2,3	– 45.0 4.0	ns OCLK Cycles
21	t_{DELLZ}	\overline{CS} High to Data 3-State	Groups 0,1,4 Groups 2,3	5.0 0.5	12.0 2.0 ns OCLK Cycles
22	t_{SUD}	Data Setup Before \overline{CS} Change		15.0	– ns
23	t_{HLDW}	\overline{AS} Hold After \overline{CS} Low	Groups 0,1,4 Groups 2,3	10.0 2.0	– ns OCLK Cycles
24	t_{DELDTL}	\overline{CS} Low to \overline{DTACK} Low	Groups 0,1,4 Groups 2,3	– 45.0 5.0	ns OCLK Cycles
25	t_{RDREC}	Read Recovery Time	Groups 0,1,4 Groups 2,3	30.0 3.0	– ns OCLK Cycles

(Sheet 2 of 2)

1. The groups referred to are the register groups shown in [Table 3.1](#) on [page 3-2](#).

8.3 L64704 Packaging

This section specifies the type of package in which the L64704 is available. [Table 8.7](#) lists ordering information for the L64704. The table and figures that follow provide three types of package information: an alphabetical pin list, a pinout, and a mechanical drawing.

Order Number	Clock Frequency (MHz)	Package Type	Operating Range
L64704B	62.5	100-pin PQFP	Commercial

Table 8.8
Alphabetical Pin List for
the 100-pin PQFP

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A0	27	$\overline{\text{CS}}$	24	RI0	11	VDD	78
A1	26	D0	43	RI1	10	VDD	86
A2	25	D1	42	RI2	9	VDD	93
$\overline{\text{AS}}$	23	D2	39	RI3	8	VDD	98
BCLKOUT	51	D3	38	RI4	7	VSS	3
CAR_DCLKN	4	D4	37	RI5	6	VSS	13
CAR_DCLKP	5	D5	36	RQ0	19	VSS	21
CAR_PED0	95	D6	35	RQ1	18	VSS	29
CAR_PED1	94	D7	33	RQ2	17	VSS	40
CAR_VCO1N	89	$\overline{\text{DTACK}}$	30	RQ3	16	VSS	46
CAR_VCO1P	91	DVALIDOUT	67	RQ4	15	VSS	52
CAR_VCO2N	88	ERROROUT	68	RQ5	14	VSS	58
CAR_VCO2P	90	FSTARTOUT	69	SDATA	44	VSS	66
CLK	22	HOST_MODE	1	SYNC/SCLK	50	VSS	72
CLK_VCON	97	IDDTN	100	VDD	2	VSS	79
CLK_VCOP	96	$\overline{\text{INT}}$	32	VDD	12	VSS	85
CO0	54	LP2	76	VDD	20	VSS	92
CO1	55	OCLK	71	VDD	28	VSS	99
CO2	56	PCLK	73	VDD	34	XCTR_IN	80
CO3	57	PLLAGND	75	VDD	41	XCTR_OUT0	81
CO4	60	PLLVD	74	VDD	47	XCTR_OUT1	82
CO5	61	PLLVSS	77	VDD	53	XCTR_OUT2	83
CO6	62	PWRP	87	VDD	59	XCTR_OUT3	84
CO7	63	READ	31	VDD	65	XOIN	48
COE	64	RESET	45	VDD	70	XOOUT	49

Figure 8.8
L64704 100-Pin PQFP
Pinout

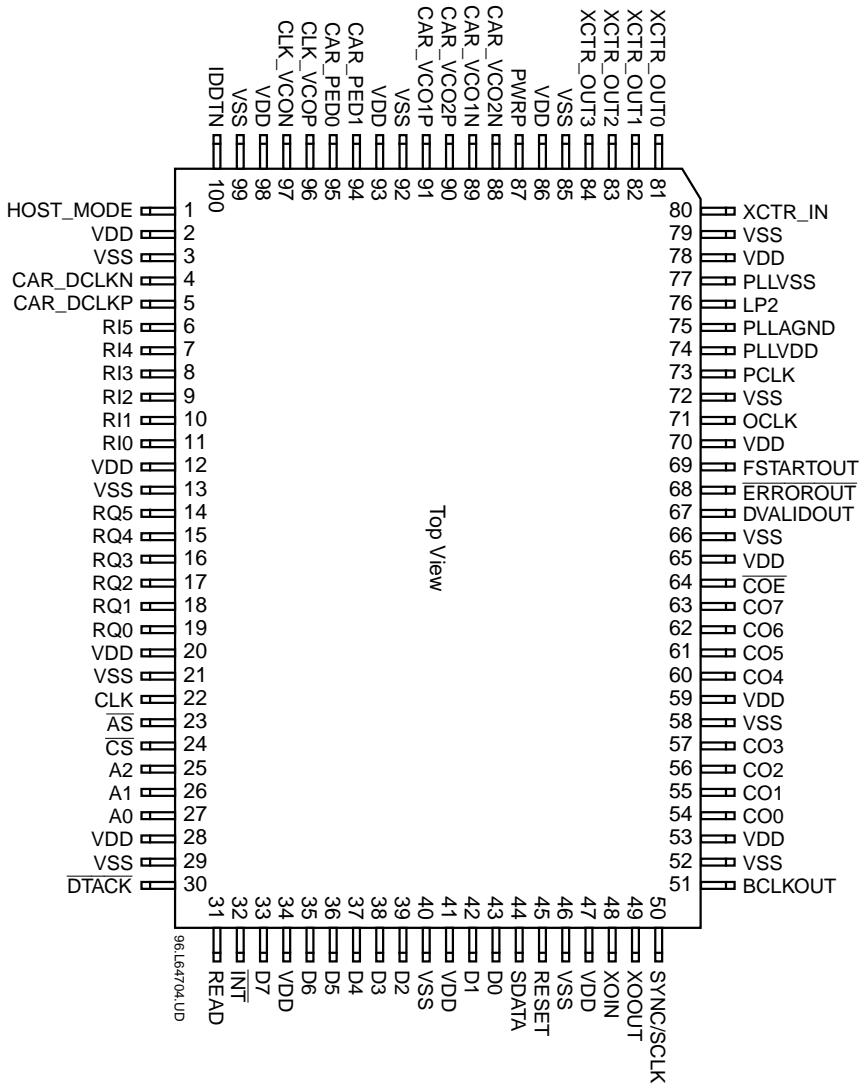


Figure 8.9
100-Pin PQFP Mechanical Drawing (Sheet 1 of 2)

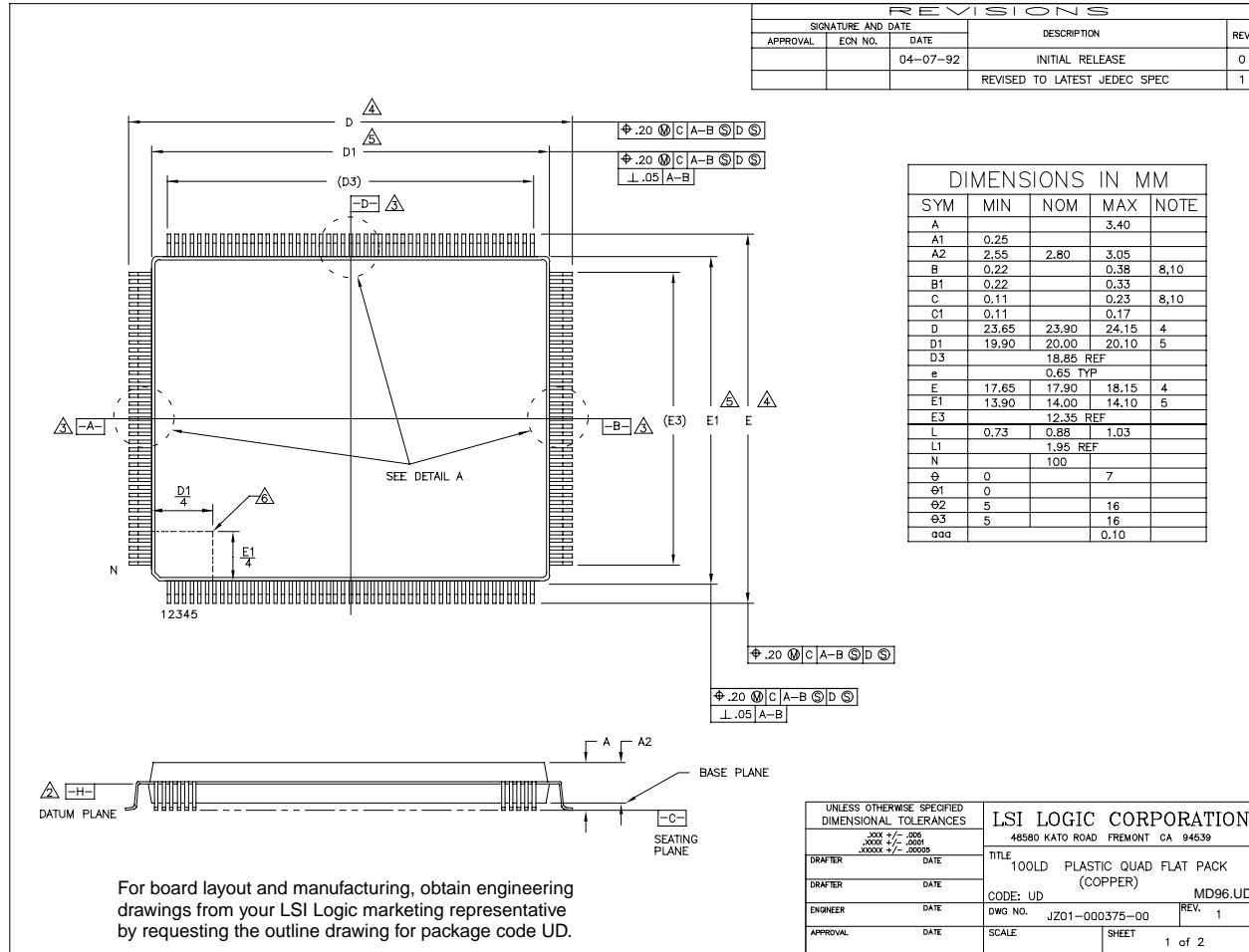
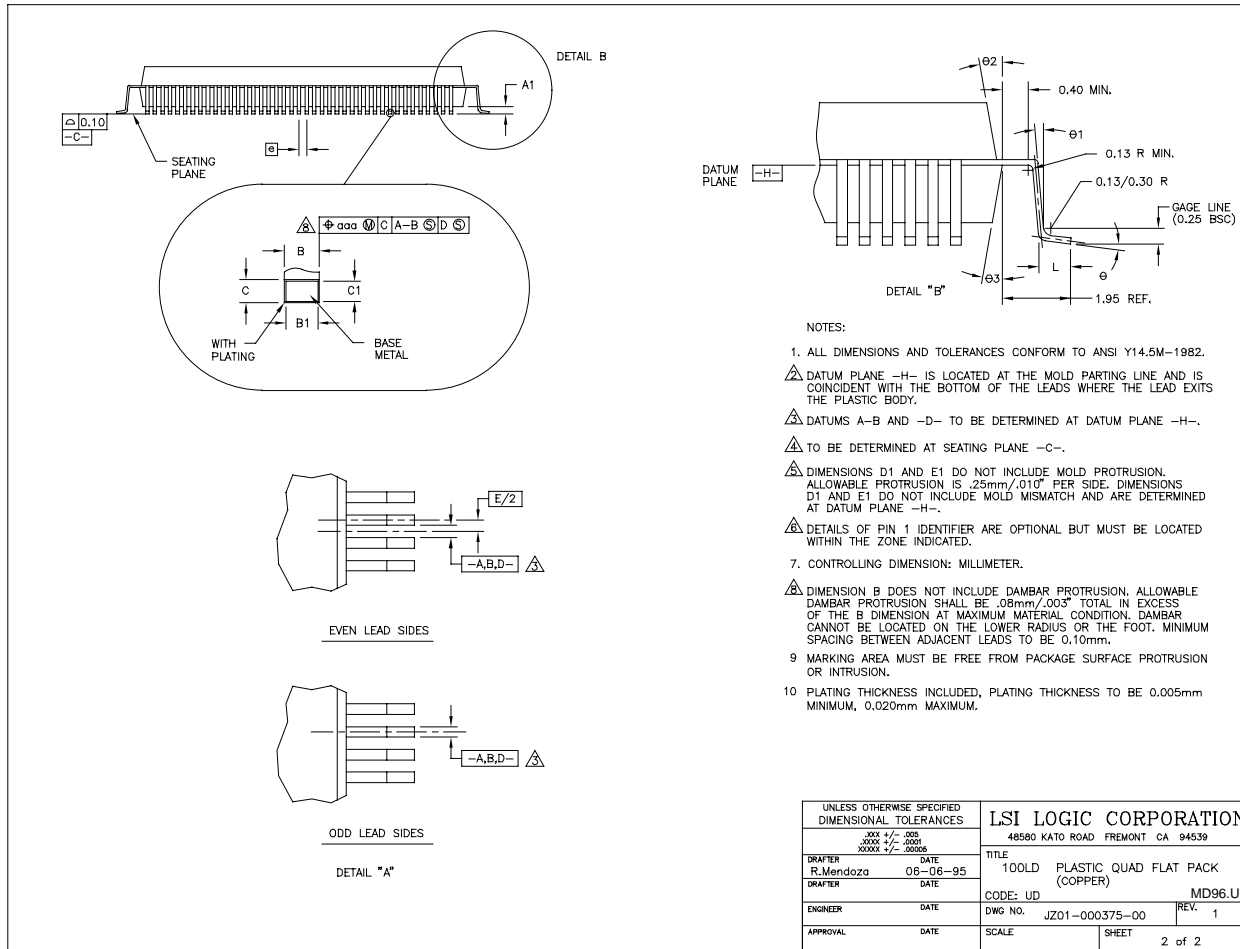


Figure 8.9 (Cont.)
100-Pin PQFP Mechanical Drawing (Sheet 2 of 2)

L64704 Packaging



8-13

Appendix A

Programming the L64704 Using the Serial Bus Protocol

This appendix discusses how to program the L64704 internal registers and data tables in Serial Host Interface mode. This chapter is intended primarily for system programmers who are developing software drivers using the serial bus.

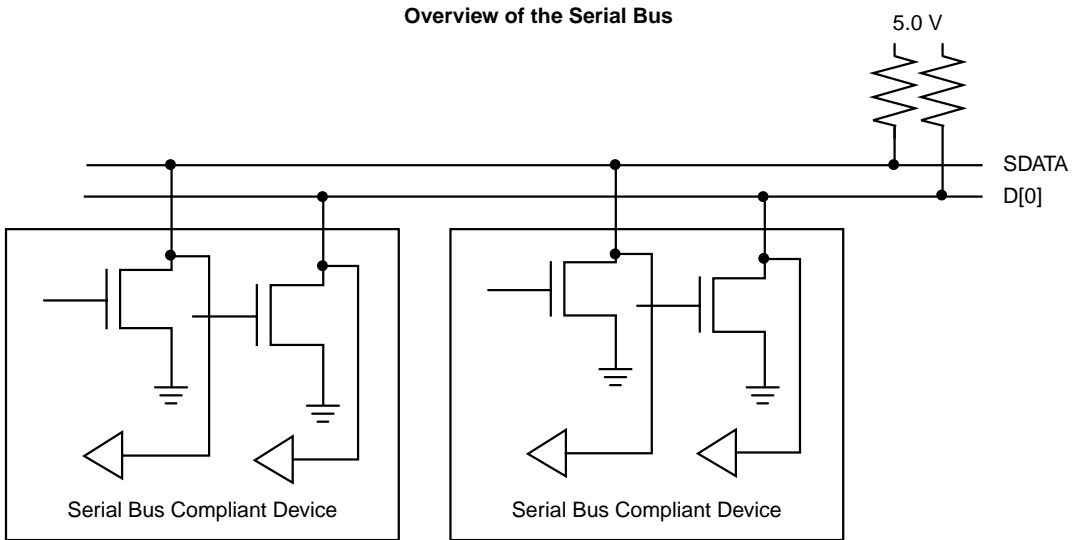
This chapter contains the following sections:

- ◆ [Section A.1, “Serial Bus Protocol Overview,”](#) provides a high-level overview of the serial bus protocol.
- ◆ [Section A.2, “Programming the Slave Address Using the Serial Bus Interface,”](#) shows how the slave address is formed and transmitted.
- ◆ [Section A.3, “Write Cycle Using the Serial Bus Interface,”](#) shows an example of a serial bus write cycle.
- ◆ [Section A.4, “Read Cycle Using the Serial Bus Interface,”](#) shows an example of a serial bus read cycle.

A.1 Serial Bus Protocol Overview

The multi-master serial bus interface has two one-bit lines – SDATA (Serial Data) and D[0] (Serial Clock) – that are connected to the bus as shown in [Figure A.1](#). External pullup resistors are used to hold the bus at a logic “1” value when the bus is not in operation.

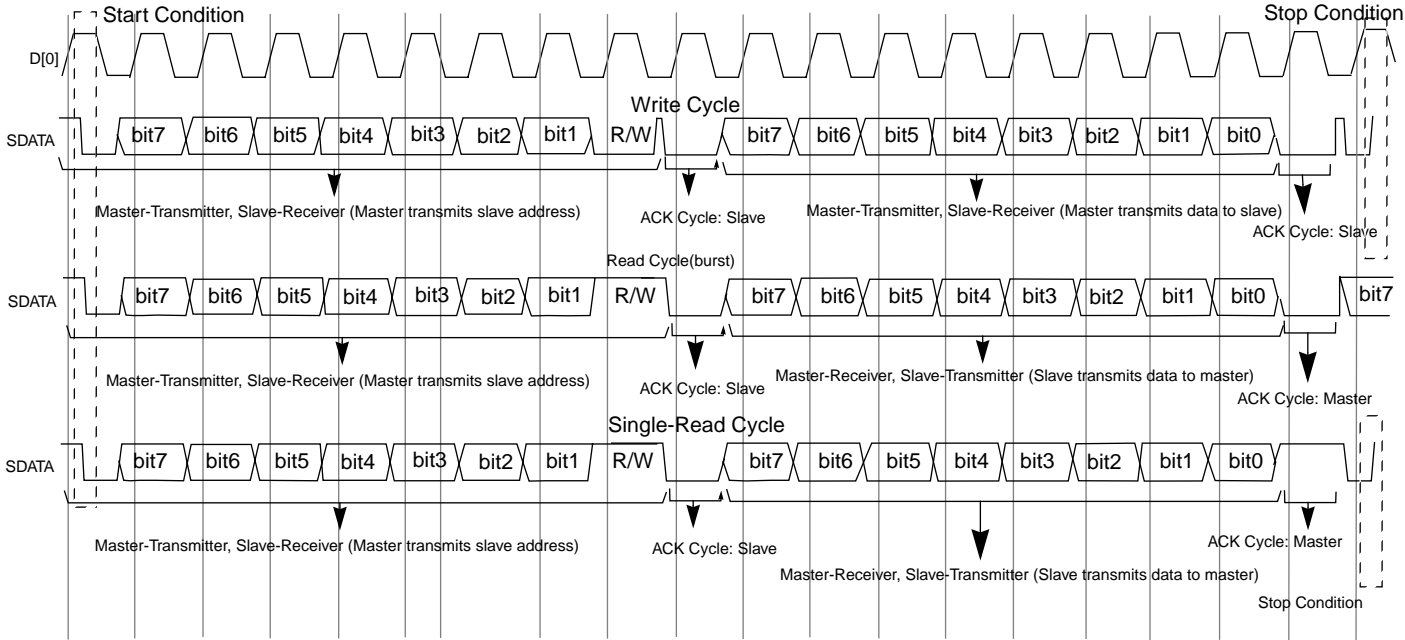
Figure A.1
Quick Overview of the
Serial Bus



Serial Host Interface mode is selected by driving the HOST_MODE input pin to LOW. In Serial Host Interface mode, data is transferred on the SDATA pin, synchronized to a serial clock that is input on the LSB of the Host Data Bus, D0. The serial data clock can have a maximum frequency of 400 kHz. The remaining Host Data Bus pins, D[7:1], are used to input the slave address that is required by the serial bus protocol.

The bus master always generates the clock and cycle start and stop conditions. [Figure A.2](#) gives an overview of the Read and the Write cycles using the Serial Bus Protocol.

Figure A.2
Quick Overview of
Serial Bus Write/Read
Cycles



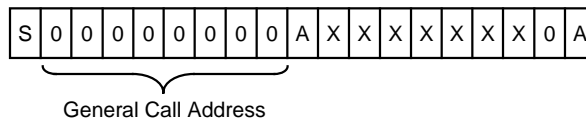
Start Condition: The master (which drives the D[0]) indicates the start of a cycle by pulling SDATA to LOW when D[0] is HIGH.
Stop Condition: The master (which drives the D[0]) indicates the end of a cycle by releasing SDATA to HIGH when D[0] is HIGH.
Data Transfer: All data changes on the SDATA line happen only when clock is LOW, except for the special cases outlined above to indicate cycle Start/Stop.
Acknowledge: The receiver always generates the acknowledge. In the case of a single read, the master-receiver does not generate an ACK so that it can generate the Stop condition (as indicated above).

A.2 Programming the Slave Address Using the Serial Bus Interface

A general call (Master does a start condition followed by eight 0's as shown in [Figure A.3](#)) address is used to address every device on the serial bus. Any device that requires information to be supplied through this general call structure should acknowledge the cycle. The second byte has the following meaning when its LSB is "0":

00000110 (0x6) Reset and write the programmable part of the slave address by hardware. For the L64704, this means reading the D[7:1] pins. (These pins are unused when the serial interface is in use, and can be hardwired to any legal 7-bit address value).

Figure A.3
General Call
Structure



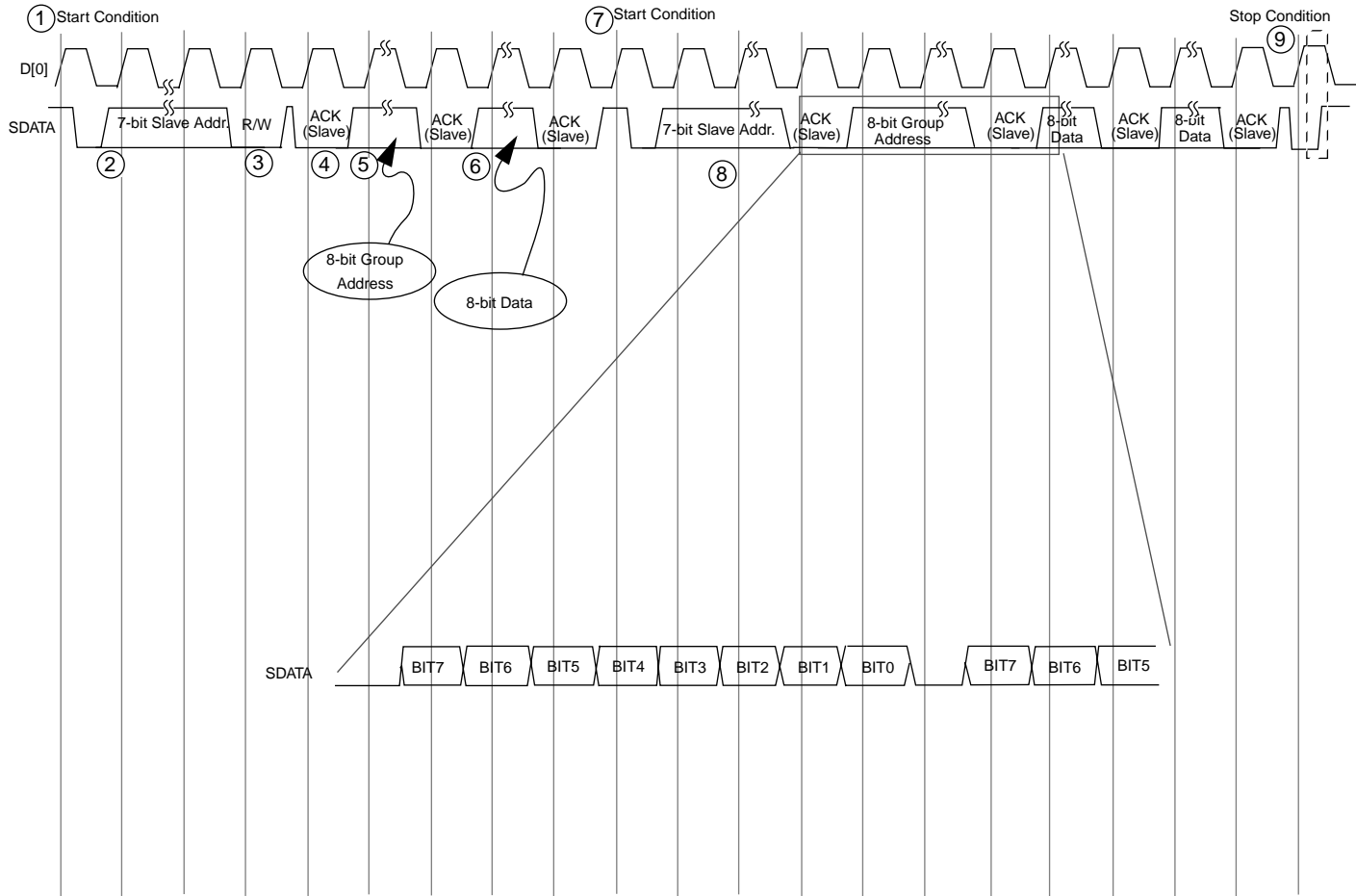
1. S = Start Condition.
2. A = Acknowledge Cycle.

A.3 Write Cycle Using the Serial Bus Interface

Refer to the following figure for a burst, or a single write cycle. The following cycles must take place for a write cycle:

1. The master starts the cycle with the start condition.
2. The master transmits the 7-bit slave address.
3. The master transmits an eighth bit (the R/W bit) = 0 to indicate a write cycle.
4. The addressed slave acknowledges the reception of the slave address by driving SDATA low in the ACK cycle.
5. The master sends the 8-bit Group 0 address (0x0) to indicate that the APR is to be loaded. (Group 0 is accessed only to load the APR).
6. The master then sends the 8-bit data. This data is used to initialize the Address Pointer register (APR0/1).
7. The master generates another start condition.
8. The master repeats steps 2-7 to address the appropriate group and write one or more data bytes.
9. The master terminates the cycle by issuing a stop condition.

Figure A.4
 Burst Write to Slave (Master-Transmitter,
 Slave-Receiver)

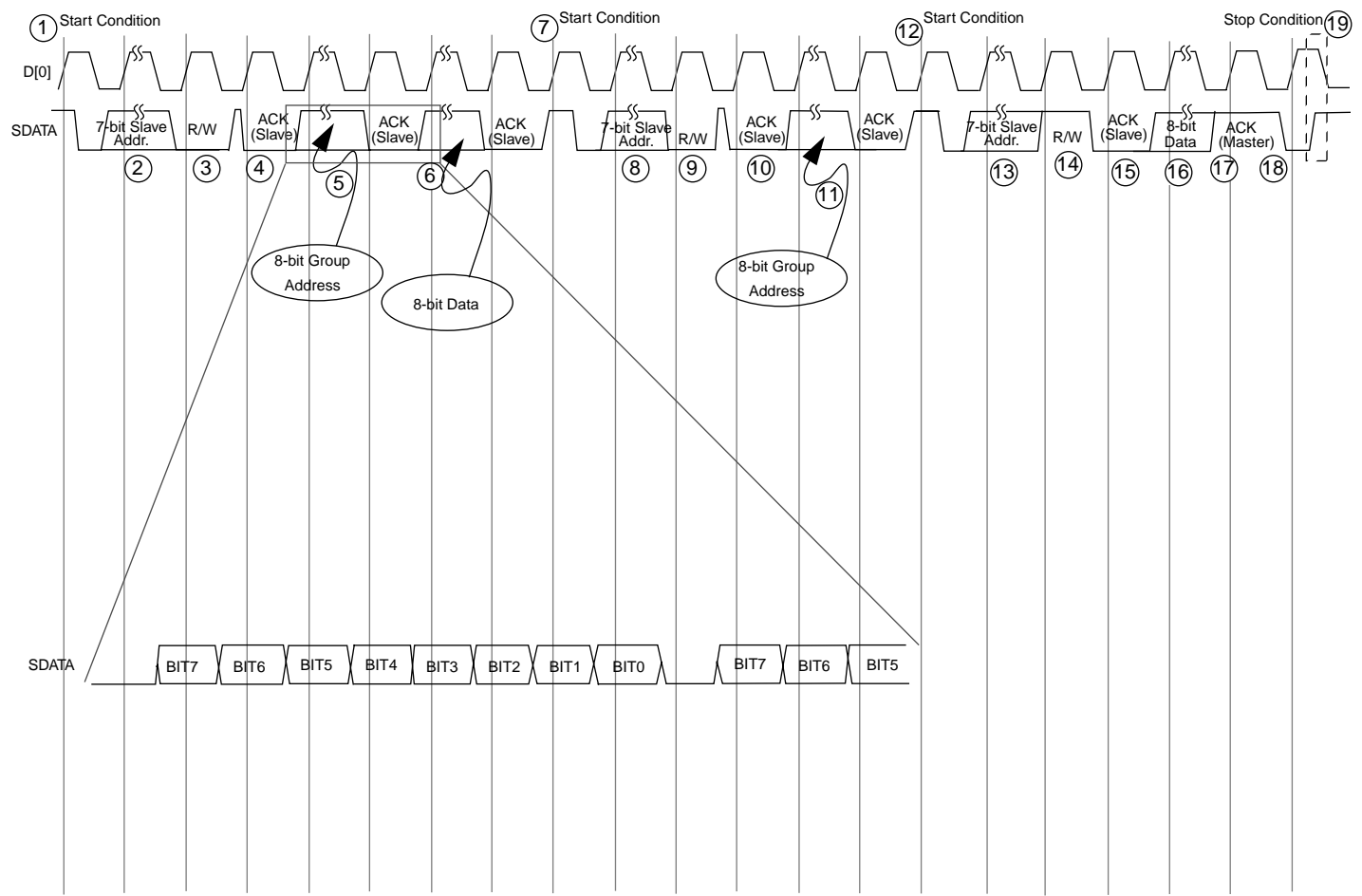


A.4 Read Cycle Using the Serial Bus Interface

Please refer to the following figure for a burst, or a single read cycle. The following cycles must take place for a read cycle:

1. The master starts the cycle by issuing a start condition.
2. The master transmits the 7-bit slave address.
3. The master sets the R/W bit = 0 to indicate a write cycle.
4. The addressed slave acknowledges the reception of the slave address by driving SDATA low in the ACK cycle.
5. The Master sends the 8-bit Group 0 address(0x0) to indicate that the APR is to be loaded. (Group 0 is accessed only to load the APR).
6. The master then sends the 8-bit data. This data is used to initialize the base pointer (APR0/1).
7. The master does a repeat start condition.
8. The master transmits the 7-bit slave address.
9. The master sets the R/W bit = 0 to indicate a write cycle.
10. The addressed slave acknowledges the reception by driving SDATA low in the ACK cycle.
11. The master transmits the number of the group that it wishes to read (which is acknowledged by the slave).
12. The master issues another start condition.
13. The master transmits the 7-bit slave address.
14. The master sets the R/W bit = 1 to indicate a read cycle.
15. The slave drives SDATA LOW to acknowledge.
16. The slave starts transmitting the data, MSB first.
17. The master has to provide the acknowledge by driving SDATA LOW during the ACK cycle.
18. In the case of a single read, the master does not drive SDATA low during the ACK cycle after reception of the first byte. The slave responds to this by relinquishing control of the bus and waiting for the master to issue a stop condition. For burst reads, the master drives SDATA low for each byte it receives during the ACK cycle, except for the last byte.
19. The master terminates the cycle by issuing a stop condition.

Figure A.5
Single Read From Slave



Read Cycle Using the Serial Bus Interface

Appendix B

L64704

Application Notes

This appendix provides updated information on the use of LSI Logic's L64704 Satellite Decoder in a typical application. It is divided into these sections:

- ◆ [Section B.1, "Controlling the L64704's BPSK/QPSK Demodulator Loops,"](#) describes how to program and monitor the L64704's AGC Clock Synchronization and Carrier Synchronization loops.
- ◆ [Section B.2, "L64704 QPSK Demodulator Debugging Tips,"](#) provides information on how to debug problems in the L64704's demodulator.
- ◆ [Section B.3, "QPSK Demodulator Configuration Example,"](#) shows an example of how the demodulator portion of the L64704 can be programmed.
- ◆ [Section B.4, "Configuring the L64704 FEC Decoder to the DVB Specifications,"](#) shows an example of how the FEC Decoder can be programmed to adhere to the DVB specifications.

B.1 Controlling the L64704's BPSK/QPSK Demodulator Loops

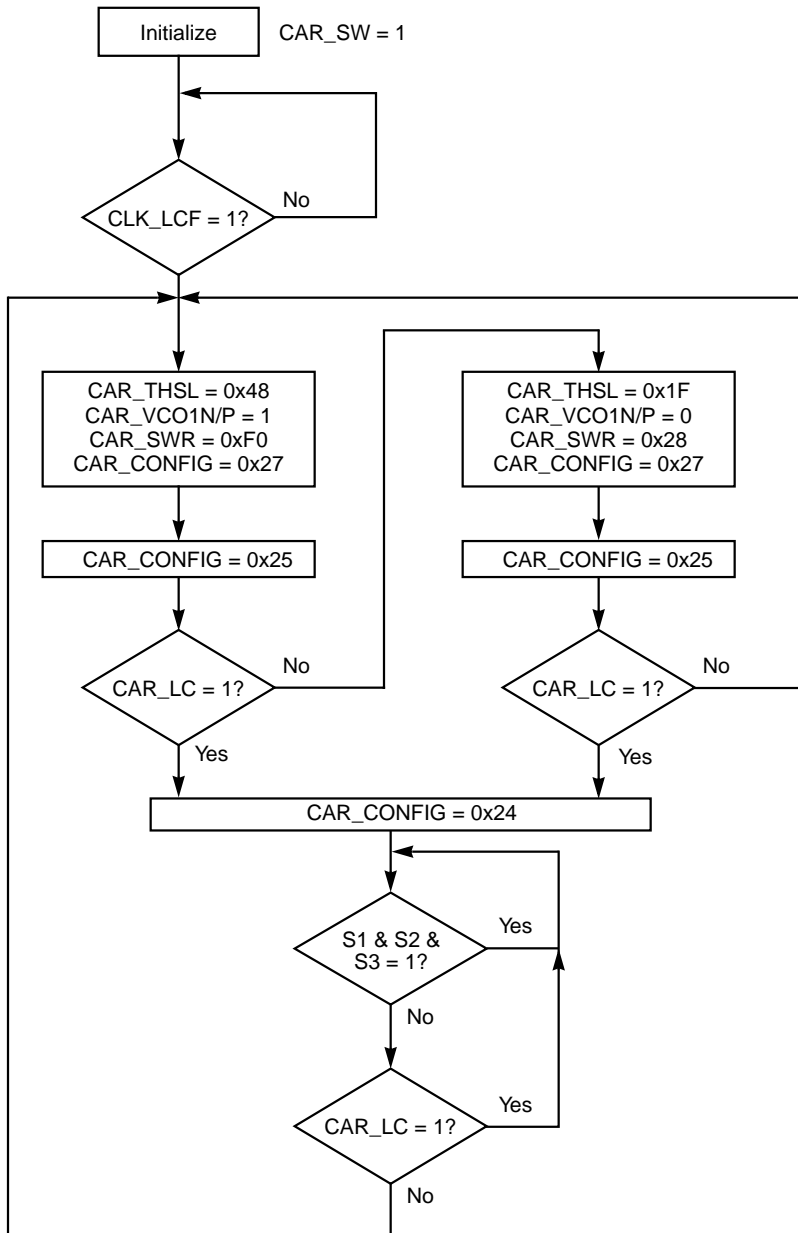
The QPSK Demodulator portion of the L64704 has three independent loops that a microcontroller must configure properly. The first loop to monitor is the AGC loop. After the microcontroller ensures the AGC loop is working, it can proceed to the Clock Synchronization and Carrier Synchronization loops. [Figure B.1](#) is a flow diagram that explains the simple process that runs on the microcontroller. You should program the microcontroller to monitor the L64704's flags.

Table B.1 shows the registers and flags that are referred to in Figure B.1.

Table B.1
QPSK
Demodulator Loop
Registers

Mnemonic	Description	Group	APR	Bit(s)
CLK_LCF	Clock Frequency Lock Flag	3	9	3
CAR_THSL	Threshold for Carrier Lock Detector	4	27	7:0
CAR_VCO1N/P	CAR_VCO1N/P Outputs Active or 3-state	4	33	4
CAR_SWR	Sweep Rate for Carrier Sweep	4	28	7:0
CAR_CONFIG	Carrier Loop Configuration Register	3	33	7:0
CAR_LC	Carrier Frequency Lock Flag	3	9	5
S1	Stage 1 (Viterbi) Synchronization Flag	3	9	0

Figure B.1
Flow Diagram of
Microcontroller
Monitoring External
Loops



B.2 L64704 QPSK Demodulator Debugging Tips

This section presents a debugging procedure to follow in case the L64704's QPSK demodulator fails to lock.

B.2.1 AGC Loop

The AGC loop must lock first. When the AGC loop is closed, the signal level at the Analog to Digital Converter's (ADC) input is 0.588 (1/1.7) times the ADC range, assuming the PWR_REF register (Group 4, APR 19) is set to 84.

A simple test that you can perform is to change the power of the transmitted signal and observe the I or Q channels with an oscilloscope just before the ADC's input. Make sure that the peak-to-peak signal range is about 1/1.7 of the peak-to-peak ADC range. Also check that the AGC can keep the signal level fixed even when the transmitted power is changed. Observe that the AGC voltage at the loop's output is changing with the changes in the transmitted power. You may need to switch the polarity of the PWRP output by toggling the PWRP bit (Group 4, APR 35).

The following parameters are related to the AGC loop:

PWR_REF[7:0]; Group 4, APR19 – This parameter controls the signal level at the input of the ADC. It should be set to 84.

PWR_LVL[7:0]; Group 3, APR 8 – This read-only register is proportional to the mean value of the sigma-delta output. If the AGC amplification range is 0 dB to -30 dB, [Table B.2](#) shows corresponding PWR_LVL settings and amplification levels.

Table B.2
PWR_LVL Register
Setting

PWR_LVL Setting	Amplification (dB)
0	0
128	-15
255	-30

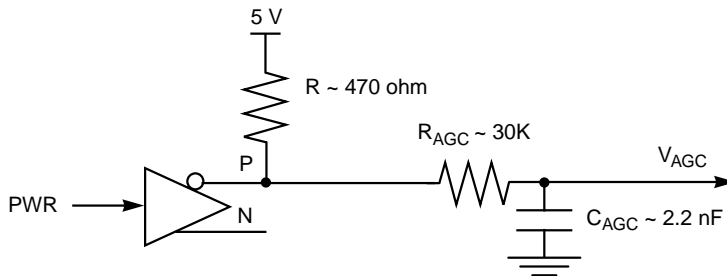
SCALE[7:0]; Group 4, APR 21 – This parameter controls the internal signals DEMI and DEMQ (see [Figure 1.1](#) on [page 1-2](#)). It does not affect the loop itself, but it is related to PWR_REF by [Equation B.1](#).

Equation B.1
$$\text{SCALE} \times \sqrt{2(\text{PWR_REF})} = 2047$$

So if PWR_REF = 84, then SCALE = 158.

PWRP Pin – Connect the L64704’s PWRP output pin to 5 volts using a 470 ohm pull-up resistor. The PWRP pin is then connected to an RC loop filter with a time constant of ~ 60 microseconds. [Figure B.2](#) shows how to connect the PWRP pin to the AGC circuit.

Figure B.2
AGC Loop Control



For more information on the AGC loop, see [Section 5.7, “Automatic Gain Control \(AGC\).”](#)

B.2.2 Clock Loop

The design of the board should keep the two $\Sigma\Delta$ (Sigma Delta) lines CLK_VCON and CLK_VCOP parallel and minimize the distance from the L64704 output to the op-amp’s input.

The microcontroller software has limited control over the clock loop. Set the loop’s bandwidth according to [Table 5.2](#) on [page 5-8](#). [Table B.3](#) shows the registers that are used to control the clock loop and [Section 5.5, “Channel Clock Recovery”](#) explains their function.

Table B.3
QPSK
Demodulator Loop
Registers

Mnemonic	Description	Group	APR	Bit(s)
CLK_LCF	Clock Frequency Lock Flag	3	9	3
	Clock Loop Control Register 1		14	7:0
	Clock Loop Control Register 2		15	7:0
CLK_NF[15:0]	Nominal Frequency of the Clock Input		16:17	7:0
CLK_RATIO[2:0]	Clock Ratio		18	

Check that the clock frequency is not stuck at the rail, and that the op-amp's output voltage is not stuck at either 0 volts or the supply voltage. The CLK_VCO_SWAP bit (Group 4, APR 14, bit 2) controls the polarity of the CLK_VCOP/N signals.

To verify that the clock loop functions, trigger the ADC clock against the BERT's clock. If the clock loop is functioning normally, then the two clocks are in phase.

The CLK_LCF status bit (Group 3, APR 9, bit 3) indicates whether the clock loop is locked. The indication is for frequency lock and the flag should be ON as soon as you finish programming the configuration (Group 4) registers.

B.2.3 Carrier Loop

The layout of the board should keep the two pairs of $\Sigma\Delta$ lines, CAR_VCOxN and CAR_VCOxP, parallel and minimize the distance from the L64704 output to the op-amp's input. The following paragraphs outline a simple test to verify that the carrier loop functions:

- ◆ Set the CAR_SW and CAR_OPEN bits in the Carrier Loop Configuration register (Group 4, APR 33) to b11. This forces the sweep to begin and disables the AFC.
 - Change the upper and lower sweep limits registers (CAR_USWL and CAR_LSWL; Group 4, APR 29:32) and watch the prescaler with a spectrum analyzer to see how the programmed values control the sweep range.
 - Change the value in the Carrier Sweep Rate register (CAR_SWR; Group 4, APR 28) to ensure that it is controlling the sweep rate.

- Set the CAR_SW and CAR_OPEN bits in the Carrier Loop Configuration register to b01 and see if the carrier locks. The microcontroller should monitor the content of the STATUS register (Group 3, APR 9). If the CAR_LC and CAR_LCF bits both = 1, then clear bits 0 and 1 of the CAR_CONFIG register to stop the sweep. If the sweep rate is fast, you may not be able to turn the sweep off fast enough through manual intervention; the microcontroller will have to do this in real time.
- ◆ If the carrier always goes to the rail, then change the CAR_SWP_SWAP and CAR_VCO_SWAP bits in the Carrier Loop Configuration register. These bits control the sweep direction and the polarity of the CAR_VCOxN/P outputs. If changing polarity does not help, disconnect the op-amp's output and drive the VCO with a power supply to see whether changing the voltage controls the frequency.
- ◆ If the prescaler output is at a proper frequency and the op-amp's output is not at the rail, look at the eye pattern to see where the data is being sampled. A good test is to trigger the ADC's I or Q inputs against the ADC's clock (see [Figure 4.1](#) on [page 4-2](#)). The clock must sample the data at the maximum eye opening.

B.2.4
QPSK
Demodulator
Debugging
Summary

The following steps summarize how to debug the QPSK Demodulator portion of a system that includes the L64704.

- Step 1. Ensure that the AGC loop functions properly.
- Step 2. Ensure that the clock loop is locked.
- Step 3. Set the CAR_SW and CAR_OPEN bits in the Carrier Loop Configuration register to b11. This setting forces sweep to begin and disables the AFC.
 - ◇ Change the Carrier Upper and Lower Sweep Limits registers (Group 4, APR 29:32) and watch the carrier prescaler with a spectrum analyzer to see how the programmed values control the sweep range.
 - ◇ Change the value in the Carrier Sweep Rate register (Group 4, APR 28) to ensure that it is controlling the sweep rate.
- Step 4. If the carrier always goes to the rail, then change the CAR_SWP_SWAP and CAR_VCO_SWAP bits in the Carrier

Loop Configuration register. These bits control the sweep direction and the polarity of the CAR_VCOxN/P outputs.

- Step 5. Set the CAR_SW and CAR_OPEN bits in the Carrier Loop Configuration register to b01. The loop should now lock or at least slow down near the center of the frequency range.
- Step 6. If the carrier still does not lock, check the following parameters:
 - ◇ CAR_KP
 - ◇ CAR_KD
 - ◇ CAR_SWR
 - ◇ Recalculate RC valuesEach one of these parameters affects the behavior of the loop.
- Step 7. If the carrier seems to lock and stops sweeping, then check the Carrier and FEC Synchronization Status register (Group 3, APR 9) for the status. All flags should be set to one when the carrier and clock are locked.
- Step 8. If all of the flags in the Carrier and FEC Synchronization Status register are set to 1, then set the CAR_SW and CAR_OPEN bits in the Carrier Loop Configuration register r to b00, This turns off the sweep.

**B.3
QPSK
Demodulator
Configuration
Example**

This section shows an example of how to configure the QPSK Demodulator section of the L64704 through its microcontroller interface. This example configuration is optimized for fixed rate operation with the following parameters:

- ◆ Transmission Rate: 42.6 Mbps (21.3 Mbaud)
- ◆ Clock VCO: 42.6 MHz (1 MHz/V)
- ◆ Carrier VCO: 479.75 MHz (1.8 MHz/V)
- ◆ Xtal OSC: 10.00 MHz
- ◆ ADC: Input: 1.0 V p-to-p
- ◆ DC offset control: not used

**B.3.1
Programming
the L64704
QPSK
Demodulator
Registers**

This subsection describes how to program each of the L64704's registers. The microcontroller addresses these registers as described in [Section 3.1, "L64704 Register Overview."](#)

Group 4, APR 14 – Set the lower four bits in the Clock Loop Control 1 register as shown in the following table.

Bits	Setting	Acronym	Meaning
1:0	0	CLK_DR[1:0]	No decimation, oversampling ratio = 2.
2	0	CLK_VCO_SWAP	CLK outputs not swapped.
3	0	CLK_LCF_Suppress	AFC enabled.

Set Group 4, APR 14 to 0x00.

Group 4, APR 15 – The recommended value for CLK_RP[3:0] is 10.

Set Group 4, APR 15 to 0x0A.

Group 4, APR 16-17 – The recommended value for CLK_NF[15:0] is 43622, as computed from [Equation 5.1](#) on [page 5-6](#):

$$\text{CLK_NF} = \frac{42.6 \times 10 \times 1024}{10} = 43622$$

Set APR 16 to 0xAA and APR 17 to 0x66.

Group 4, APR 18 – The recommended value for CLK_RATIO[2:0] is 0 for only 2 samples/symbol.

Set Group 4, APR 18 to 0x00.

Group 4, APR 19 – PWR_REF[7:0] = 84 is the recommended value if L = 1. As discussed in [Section 5.7.1, "ADC Range and Power Reference,"](#) 2R is the ADC range p-to-p and 2S is the input signal range p-to-p on the I and Q channels. The ratio S:R must be 1:1.7 when PWR_REF = 84.

$$\frac{S}{R} = \frac{1}{1.7}$$

So, in this case the input signal level is

$$S = \frac{0.5 \times 1.0}{1.7} = 0.29.$$

If the AGC loop is not connected, ensure that the L64704 is sending the correct output power.

Set Group 4, APR 19 to 0x54.

Group 4, APR 20 – Set PWR_BW according to [Table 5.5](#) on [page 5-23](#). PWR_BW[1:0] = 0 in this example.

Set Group 4, APR 20 to 0x00.

Group 4, APR 21 – The recommended value for SCALE[7:0] is 158.

Set Group 4, APR 21 to 0x9E.

Group 4, APR 22 – Set SNR_THS[7:0] = 0x1F.

Set Group 4, APR 22 to 0x1F.

Group 4, APR 23 – Set CAR_OFFSET[7:0] = 0.

Set Group 4, APR 23 to 0x00.

Group 4, APR 24 – The recommended value for CAR_RP is 8.

Set Group 4, APR 24 to 0x08.

Group 4, APR 25 – Set CAR_KP to 64. The CAR_KP register has a limited range between 30 and 127; values above 127 do not work.

For fixed rate operation:

- ◆ Select B_L (the equivalent noise BW) based on the criteria shown in [Equation B.2](#) and [Table B.4](#):

Equation B.2

$$B_L = 0.001 \times \text{BaudRate}$$

$$B_L = \frac{\omega_n}{2} \left(\xi + \frac{1}{1 + 4\xi} \right)$$

Where ζ is the loop's damping, ω_n is in rad/s, and B_L is in Hz.

Table B.4
 ω_n for Fixed Rate
 Operation
 (Damping = 1)

Data Rate (Mbaud)	ω_n (kilorad/s/volt)
10	16
20	32
30	48

- ◆ Set CAR_KP to 0X40. Because of the limited range of CAR_KP (30 and 127) This value places it in the middle of the range.
- ◆ Based on [Equation 5.11](#) on [page 5-18](#),

$$R_{CAR}C_{CAR} = \frac{3.3K_D K_{CARVCO}}{CAR_KP \omega_n^2}$$

K_D is the Phase Detector Gain and it depends on whether the DDML or the NDAML estimator is selected (CON_SEL; Group 4, APR 35). [Figure 5.9](#) on [page 5-19](#) shows the Gains of the two phase detectors as a function of C/N.

K_D is about 10 for C/N = 4 dB (Channel Eb/No = 1 dB).

Set $K_D = 10$, $K_{CARVCO} = 1.8 \text{ MHz/V} = 11.3 \text{ Mrad/s/V}$ and $\omega_n = 32 \text{ K Rad/s/v}$.

$$R_{CAR}C_{CAR} = \frac{3.3 \times 10 \times 1.8 \times 10^6 \times 2\pi}{64(32 \times 10^3)^2}$$

Therefore in this example, $R_{CAR}C_{CAR} = 10 \text{ ms}$.

Group 4, APR 26 – The recommended value for CAR_KD is 207, based on [Equation 5.11](#) on [page 5-18](#),

$$CAR_KD = \frac{\zeta}{2\omega_n T} = 207$$

where $\zeta = 1$, $\omega_n = 51.5 \text{ krad/s/V}$, and $T = 2/42.6 \times 10^6$.

Set Group 4, APR 26 to 0xCF.

Group 4, APR 27 – The recommended value for CAR_THSL[7:0] is 31 when FP_LOCK_LEN (Group 4, APR 35) is set to 0. Otherwise, set it according to the following table:

FP_LOCK_LEN	CAR_THSL[7:0]	Signal to Noise Ratio
0	31	Low Eb/No
1	72	High Eb/No

Set Group 4, APR 27 to 0x1F.

Group 4, APR 28 – The recommended starting point for CAR_SWR[7:0] is 33. Experiment with other values to optimize performance.

Set Group 4, APR 28 to 0x21.

Group 4, APR 29-30 – The recommended value for CAR_USWL[13:0] is 12301, assuming that the prescaler divides the frequency of the carrier VCO by 32 and that jitter is ± 1 MHz.

$$\text{CAR_USWL} = ((479.5 + 1) / 32) \times ((8 \times 1024) / 10) = 12301$$

Set APR 29 to 0x30 and APR 30 to 0x0D.

Group 4, APR 31-32 – Set CAR_LSWL to 12250, based on the following equation:

$$\text{CAR_LSWL} = ((479.5 - 1) / 32) \times ((8 \times 1024) / 10) = 12250$$

Set APR 31 to 0x2F and APR 32 to 0xDA.

Group 4, APR 33 – Set the Carrier Loop Configuration register to 0x25 when this register's bits are set as shown in the following table.

Bit	Setting	Meaning
0	1	Carrier sweep on
1	0	CAR_OPEN. Set to one only to get out of false lock
2	1	0 = DDML, 1 = NDAML
3	0	0 = Sigma Delta, 1 = 6-bit output to DAC
4	0	CAR_VCO1N/P, 0 = active, 1 = 3-state
5	1	CAR_VCO2N/P, 0 = active, 1 = 3-state
6	0	CAR_VCOxN/P output polarity, 0 = normal, 1 = swapped
7	0	Sweep Direction, 0 = normal, 1 = swapped

Together, bits 6 and 7 may be set to any one of four values. Use the following guidelines for programming these bits:

1. If the carrier frequency sweep gets stuck at the upper or lower rail, change the polarity of the bits until the sweep works correctly.
2. If the carrier is locked but the constellation is rotated by 45 degrees, reverse the polarity of each bit.

Set Group 4, APR 33 to 0x25. When the Carrier and FEC Synchronization Status register (Group 3, APR 9) indicates a lock, change it to 0x24.

Group 4, APR 34 – Set to 0 – All of the bits in this register must be set to 0 for proper operation.

Group 4, APR 35 – The settings in the Decoder Configuration register are application dependent. Do not use the SNR estimator in this example.

Group 3, APR 6-7 – CAR_VCOF[13:0] = shows the result of the VCO frequency measurement. The resolution of the received value depends on the prescaler as shown in the following table.

Prescaler Divisor	Δf_{VCO} (kHz)
16	19.5
32	39

Group 3, APR 9 – STATUS[2:0] is a read-only register.

Table B.5 shows a register map of the register used to configure the BPSK/QPSK demodulator portion of the L64704, and Table B.6 provides a summary of all of the programming information supplied above.

Table B.5
Group 4 Decoder
Register Map

APR[5:0]	D7	D6	D5	D4	D3	D2	D1	DO
14	SYNC/ SCLK	Reserved	Set to 0	F_OUT_ HiZ	CLK_LCF_ SUPPRESS	CLK_VCO_ SWAP	CLK_DR[1:0]	
15	Set to 0	PCLK_BP	Set to 0	PD	CLK_RP			
16	CLK_NF[15:8]							
17	CLK_NF[7:0]							
18	Reserved					CLK_RATIO[2:0]		
19	PWR_REF[7:0]							
20	Reserved					INT_DC	PWR_BW[1:0]	
21	Scale Factor for DEMI, DEMQ, SCALE[7:0]							
22	SNR Estimator Threshold, SNR_THS[7:0]							
23	Carrier Loop DC Offset Compensation, CAR_OFFSET[7:0]							
24	Reserved				Carrier Reference Period, CAR_RP[3:0]			
25	Carrier Loop Filter Gain (P Term), CAR_KP[7:0]							
26	Carrier Loop Filter Gain (D Term), CAR_KD[7:0]							
27	Carrier Lock Detector Threshold, CAR_THSL[7:0]							
28	Carrier Sweep Rate, CAR_SWR[7:0]							
29	Reserved		Carrier Upper Sweep Limit, CAR_USWL[13:8]					
30	Carrier Upper Sweep Limit, CAR_USWL[7:0]							
31	Reserved		Carrier Lower Sweep Limit, CAR_LSWL[13:8]					
32	Carrier Lower Sweep Limit, CAR_LSWL[7:0]							
33	CAR_SWP_ SWAP	CAR_VCO_ SWAP	CAR_VCO2 N/P	CAR_VCO1 N/P	CAR_OUT_ SEL	CAR_PED_ SEL	CAR_OPEN	CAR_SW
34	Set to 0				Reserved			
35	SNR_EST	CON_SEL	Set to 0	FP_LOCK_ LEN	PWRP	Set to 0		I_FORMAT
36	Reserved		External Control Output Bits, XCTR[3:0]				DEMOD_ RST	FEC_RST

Table B.6
 Group 4 Decoder
 Registers Actual
 Configuration

APR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
14	0	0	0	0	0	0	0	0	00
15	0	0	0	0	1	0	1	0	0A
16	1	0	1	0	1	0	1	0	AA
17	0	1	1	0	0	1	1	0	66
18	0	0	0	0	0	0	0	0	00
19	0	1	0	1	0	1	0	0	54
20	0	0	0	0	0	0	0	0	00
21	1	0	0	1	1	1	1	0	9E
22	0	0	0	1	1	1	1	1	1F
23	0	0	0	0	0	0	0	0	00
24	0	0	0	0	1	0	0	0	08
25	0	1	0	0	0	0	0	0	40
26	1	1	0	0	1	1	1	1	CF
27	0	0	0	1	1	1	1	1	1F
28	0	0	1	0	0	0	0	1	21
29	0	0	1	1	0	0	0	0	30
30	0	0	0	0	1	1	0	1	0D
31	0	0	1	0	1	1	1	1	2F
32	1	1	0	1	1	0	1	0	DA
33	0	0	1	0	0	1	0	1	25
34	0	0	0	0	0	0	0	0	00
35	Application Dependant								N/A
36	Application Dependant								N/A

B.3.2 RC Values for Clock Loop

To compute the RC values for the clock loop using [Equation 5.3](#) and [Equation 5.4](#) on [page 5-7](#), choose the natural frequency ω_n according to [Table 5.2](#) and set the damping factor ζ to 1 for fixed rate operation.

This example uses the following values for each parameter: $\zeta = 1$, $M = 2$, $\omega_n = 3900$, and $K_{VCO} = 1$ MHz/V (assuming $K_D = 0.92$). From [Equation 5.3](#) and [Equation 5.4](#), the RC values in this example are:

$$R_{CLK2}C_{CLK} = \frac{2\zeta}{\omega_n} = 5 \times 10^{-4} \text{ seconds}$$

$$\begin{aligned} R_{CLK1}C_{CLK} &= \frac{1}{\omega_n^2} \times \frac{K_D 2\pi K_{VCO}}{2\pi M} \\ &= \frac{1}{(3.9 \times 10^3)^2} \times \frac{(0.92) 2\pi \times 10^6}{2\pi(2)} \\ &= 30 \times 10^{-3} \text{ seconds} \end{aligned}$$

Choose: $C_{CLK} = 1$ F, $R_{CLK1} = 30$ k, $R_{CLK2} = 510\Omega$.

B.3.3 VCO Gains

[Table B.7](#) gives typical ranges for the clock and carrier VCO gains. The values depend on whether your application requires fixed rate or variable rate operation.

Table B.7
Typical Clock and
Carrier VCO Gains

External Loop	VCO Gain (kHz/V)
Clock	100 to 2000
Carrier	750 to 2500

B.3.4 Low Data Rates

When the system functions at low baud rates (generally below 5 Mbaud), connect the Phase Error Detector outputs to an external DAC, and feed the voltage level from the output of the DAC to one of the loop filters as shown in [Figure 5.10](#).

The lower two bits of the Phase Error Detector outputs are brought out on the CAR_PED0 and CAR_PED1 pins. The upper four bits of the Phase detector output are shared with the four CAR_VCO pins as shown in [Table B.8](#):

Table B.8

CAR_PED Output Pin Name	CAR_OUT_SEL Bit	
	0	1
CAR_PED0	CAR_PED0	CAR_PED0
CAR_PED1	CAR_PED1	CAR_PED1
CAR_VCO1P	CAR_VCO1P	CAR_PED2
CAR_VCO2P	CAR_VCO2P	CAR_PED3
CAR_VCO1N	CAR_VCO1N	CAR_PED4
CAR_VCO2N	CAR_VCO2N	CAR_PED5

To enable the Phase Error Detector outputs, set the CAR_PED_SEL bit in the Carrier Loop Configuration register (Group 4, APR 33) to 1.

1. Choose CAR_KD.
2. Choose ζ .
3. Choose ω_n .
4. Calculate R_2 , R_1 , and C from the following equations:

$$\zeta = \frac{R_2 C \omega_n}{2}, \quad \omega_n = \sqrt{\frac{K_D K_{carvco} (\text{CAR_KD}) (\text{ADR})}{R_1 C \times 8192}}$$

where ADR is one side of the DAC range. For example, if the DAC output range is ± 1 volt, then ADR = 1.

$$\frac{2b_2}{2N - (1 + \beta)} \leq \frac{1}{T} \leq \min\left(\frac{2b_1}{1 + \beta}, \frac{f_{max}}{N}\right).$$

**B.4
Configuring the
L64704 FEC
Decoder to the
DVB
Specifications**

This section presents the steps required to configure the L64704 to the DVB specifications. The following pages continue the initialization example for the following case:

- ◆ Transmission Rate: 42.6 Mbps (21.3 Mbaud)
- ◆ QPSK Clock VCO: 42.6 MHz
- ◆ Viterbi Rate: 1/2
- ◆ ICLK: 21.3 MHz
- ◆ OCLK: 21.3 MHz

Table B.9 is the address map for the group 4 registers. Table B.10 presents the proper configuration for the above system parameters.

Table B.9
Group 4 Register Map

APR	D7	D6	D5	D4	D3	D2	D1	DO
0	Set to 1	Set to 0	PLL_N					
1	Set to 0	Set to 0	PLL_S					
2	IMQ	Set to 1	QB	PLL_T				
3	Viterbi Code Rate[2:0]		TEI	Set to 0	Set to 0	PLL_M[1:0]		
4	Viterbi Max Data Bit Count 1, VMDC1[7:0]							
5	Viterbi Max Data Bit Count 2, VMDC2[7:0], Low Byte							
6	Viterbi Max Data Bit Count 2, VMDC2[15:8], Middle Byte							
7	Viterbi Max Data Bit Count 2, VMDC2[23:16], High Byte							
8	Viterbi Maximum Bit Error Count[7:0]							
9	Synchronization Word[7:0]							
10	BER	Reserved					L[1:0]	
11	BF	Set to 0	Sync Status Select, SSS[1:0]		Sync States Acq. SSA[1:0]		Sync States Track, SST[1:0]	
12	BPS[2:0]			Set to 0	OF	Output Selector, OS[2:0]		
13	PLL_RESET							

Table B.10
Group 4 Actual
Configuration

APR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	1	0	0	0	0	0	1	0	82
1	0	0	0	0	0	1	0	0	04
2	1	1	0	0	0	0	1	0	C2
3	0	0	0	0	0	0	0	0	00
4	0	1	0	0	0	0	0	0	40
5	0	0	0	0	0	0	0	0	00
6	0	0	0	0	0	0	0	0	00
7	0	0	0	0	1	1	1	1	0F
8	0	0	0	1	1	0	0	1	20
9	0	1	0	0	0	1	1	1	47
10	0	0	0	0	0	0	0	1	01
11	1	0	0	0	0	0	0	1	81
12	0	0	0	0	0	1	0	1	05
13	0	0	0	0	0	0	0	0	00

The following paragraphs describe how to program each of the L64704's registers.

From [Table 4.2](#) on [page 4-8](#) for rate 1/2 ICLK = PCLK = 21.3 MHz, select the eighth row from the top: PLL_N = 2, PLL_S = 4, PLL_T = 2, PLL_M = 0.

Group 4, APR 0 – Set bit D7 to 1 and set bit D6 to 0. Based on line 8 from [Table 4.2](#), set the PLL_N field to 2.

Set Group 4, APR 0 to 0xC2.

Group 4, APR 1 – Set bits D7 and D6 to 0. Based on line 8 from [Table 4.2](#), set PLL_S to 4.

Set Group 4, APR 1 to 0x04.

Group 4, APR 2 – Set IMQ to either 0 or 1, the D6 bit to 1, and QB to 0 for QPSK. Based on line 8 from [Table 4.2](#), set PLL_T to 2.

Set Group 4, APR 2 to 0x42.

Group 4, APR 3 – Set VCR to 0 for rate 1/2, TEI to 0 or 1, TM to 0. Based on line 8 from [Table 4.2](#), set PLL_M to 0.

Set Group 4, APR 3 to 0x00.

Group 4, APR 4 – From the graphs starting with [Figure 7.6](#) on page [page 7-9](#), choose a value between the in-sync and out of sync curves. A value of 20% is a reasonable choice for operation at Eb/No of 3.5 and above. Based on this choice, set VMDC1 to 64 (0x40). This value selects a window of size $64 \times 256 = 16,384$ bits.

Set Group 4, APR 4 to 0x40.

Group 4, APR 5-7 – VMDC2 selects a second window. This value controls the window size over which Viterbi Errors are counted. It is used for calculating the BER, not for the auto-synchronization that is controlled by VMDC1. In this example, choose a window size of 3.932×10^6 bits = VMDC2 x 4. Other values may work as well.

Set Group 4, APR 5 to 0x00, set Group 4, APR 6 to 0x00, and set Group 4, APR 7 to 0x0F.

Group 4, APR 8 – VMSEC is the second parameter that controls the Viterbi auto-sync. Select a ratio of 20% from the value of VMDC1 x 256. $0.2 \times 16,384 = 3277$. Program the value of VMSEC to $(3277 - 32) / 128 = 25 = 0x19$.

For lower Eb/No, a ratio of 25% is better. In this case, the calculation is: $0.25 \times 16,384 = 4096$. So, the value is 32 (0x20).

Set Group 4, APR 8 to 0x20.

Group 4, APR 9 – The DVB sync word is 0x47.

Set Group 4, APR 9 to 0x47.

Group 4, APR 10 – In this example, select a value of 1. See the description of Group 4, APR 10 on [page 3-33](#).

Set Group 4, APR 10 to 0x01.

Group 4, APR 11 – In this example, select SSS = 0 to observe the Viterbi sync status. See the description of Group 4, APR 11 on [page 3-34](#).

Set Group 4, APR 11 to 0x81.

Group 4, APR 12 – This example does not use the Viterbi bypass mode, so BPS has no effect here. Set IS to 0, OF to 0, and OS to 5 to start debugging by looking at the Viterbi output.

Set Group 4, APR 12 to 0x05.

Group 4, APR 13 – Write any value to Group 4, APR 13 to reset the PLL module.

Set Group 4, APR 13 to 0x00.

Appendix C

Oscillator Cells

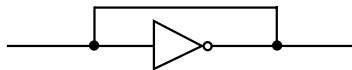
This appendix describes the LSI Logic oscillator cells used in the L64704. These cells are designed to be used with external components to form an oscillator circuit.

C.1 Introduction

Oscillator cells exist at LSI Logic in both Channel-Free Arrays and Cell-Based ASIC technologies. These cells have been designed to work with external crystals and RLC components. Passive component values on semiconductor ICs are far too variable to provide the accuracy required to obtain stable oscillation frequencies.

The simplest oscillator consists of an inverting gate with the output connected to the input as shown in [Figure C.1](#).

Figure C.1
Simplest Oscillator



Most designers avoid this type of oscillator, because its frequency is too dependent on wafer processing variations, bias voltage values, and temperature effects. The oscillator in [Figure C.1](#) is most commonly found when unwanted, positive feedback paths creep into a design, causing the apparent effect shown.

C.2 Requirements For Oscillator Circuits

The following requirements must be met for the oscillator circuits to operate properly:

- ◆ The V_{DD} ramp time must be greater than or equal to 1 millisecond to start up the oscillator.
- ◆ The EN pin must be tied to V_{DD} . This means that the EN pin cannot be used to enable or disable the oscillator.

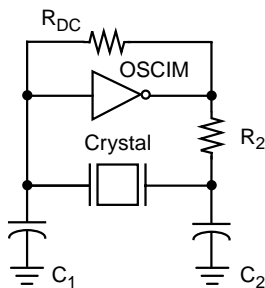
C.3 0 to 20 MHz Crystal Oscillator

LSI Logic's OSCXX cells are intended to be used with external components to form an oscillator circuit, such as the one shown in [Figure C.2](#).

The recommended crystal is an AT-cut crystal. The inherent characteristics of such a crystal produce a fundamental frequency (f_F) less than 20 MHz and third overtone frequencies (f_{3OT}) between 20 MHz and 60 MHz. Oscillation begins when the power is turned on.

Crystals by nature are usually immune to power supply and temperature variations, thereby providing very stable frequencies over the V_{DD} and T_A ranges of the ASIC devices. In addition, the duty cycle of the output waveform for the circuit in [Figure C.2](#) approaches the ideal of 50%, producing a clean symmetrical waveform.

Figure C.2
Pierce Crystal
Oscillator Circuit



1. R_{DC} = the DC resistance of the crystal. R_{DC} should be in the range from 1 to 5 Meg ohms.

For frequencies within the range of the crystal's fundamental frequency (0 to 20 MHz), the circuit in [Figure C.2](#) works with the component values given in [Table C.1](#). For the capacitors:

$$C_1 = C_2 = 2 \times C_L - C_B$$

where C_L = Crystal Parameter (typically 32 pF) and C_B = board connection capacitance (typically 3 pF).

The basis for the values in [Table C.1](#) comes from the relationship:

$$f_F \cong 1 / (2\pi R_2 \times C_2)$$

where f_F is the desired frequency of oscillation (shown on the crystal itself).

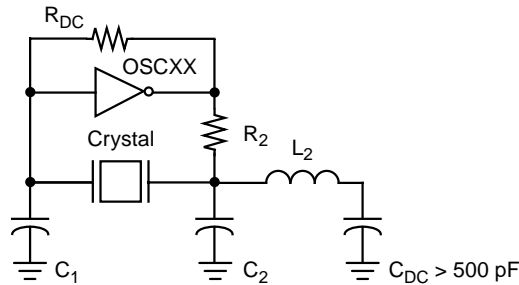
Table C.1
Component Values
for the
Circuit Shown in
[Figure C.2](#)

Frequency	$C_1 = C_2$ (pF)	R_2 (Ω)
2 MHz	61	1000
5 MHz	61	500
10 MHz	61	250
20 MHz	61	100

C.4 Higher Frequency Oscillators

Frequency ranges between 20 MHz and 60 MHz can be obtained with the circuit shown in [Figure C.3](#).

Figure C.3
A Third Overtone
(Higher Frequency)
Oscillator Circuit



1. R_{DC} = the DC resistance of the crystal. R_{DC} should be in the range from 1 to 5 Meg ohms.

Values are chosen for the components in [Figure C.3](#) based on the following considerations:

$$C_1 = C_2 = 2 \times C_L - C_B$$

where C_L = Crystal Parameter (typically 22 to 25 pF) and C_B = board connection capacitance (typically 3 pF).

$$f \cong 1 / (2\pi R_2 \times C_2) \text{ and}$$

$$f \cong 3 / (4\pi \sqrt{L_2 \times C_2})$$

where f is the desired frequency specified on the crystal. [Table C.2](#) shows typical component values for a range of frequencies.

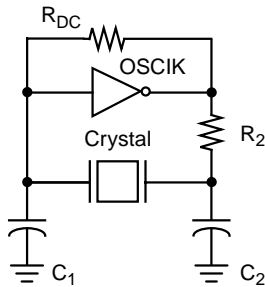
Table C.2
Component Values
for the Circuit
Shown in
[Figure C.3](#)

Frequency	C_2 (pF)	R_2 (Ω)	L_2 (μ H)
25 MHz	47	120	1.9
32 MHz	47	100	1.2
40 MHz	47	80	0.8
50 MHz	47	60	0.5

C.5 Low Frequency Oscillation (kHz Range)

A circuit that can be used to reliably obtain a lower frequency oscillation is shown in [Figure C.4](#). This circuit should be used for the 0 to 100 kHz range of frequencies.

Figure C.4
A Low Frequency
Range (kHz)
Oscillator Circuit



1. R_{DC} = the DC resistance of the crystal. R_{DC} should be in the range from 1 to 5 Meg ohms.

For the capacitors:

$$C_1 = C_2 = 2 \times C_L - C_B$$

where C_L = Crystal Parameter (typically 32 pF) and C_B = board connection capacitance (typically 3 pF).

The basis for the values in [Table C.3](#) comes from the relationship:

$$f_F \cong 1 / (2\pi R_2 \times C_2)$$

where f_F is the desired frequency of oscillation (shown on the crystal itself).

Table C.3
Component Values
for the Circuit
Shown in
[Figure C.4](#)

Frequency	C_2 (pF)	R_2 (k Ω)
20 kHz	61	100
50 kHz	61	40
75 kHz	61	25
100 kHz	61	15

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